DATA SHEET

旭曜科技 ORISE TECH

OTM4001A

720-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

DEC. 28, 2009

Version 0.5

Table of Contents

PAGE

720-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The OTM4001A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx432 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM4001A is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in OTM4001A can support several interfaces for the diverse request of medium or small size portable display. OTM4001A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the OTM4001A incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The OTM4001A also supports eight-color mode and standby mode for power saving consideration.

2. FEATURES

- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx432, incorporating a 720-channel source driver and a 432-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 233,280 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- Built-in CABC function with output control backlight pin
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Varies RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (Vcc): 2.5 ~ 3.6 V
  - I/O interface supply voltage (IOVcc): 1.65 ~3.6 V
  - Analog power supply voltage (Vci): 2.5 ~ 3.6 V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)

    VGH = 10.0V ~15.0V

    VGL = -4.5V ~ -12.5V

    VGH – VGL $\leqq$ 30.0V

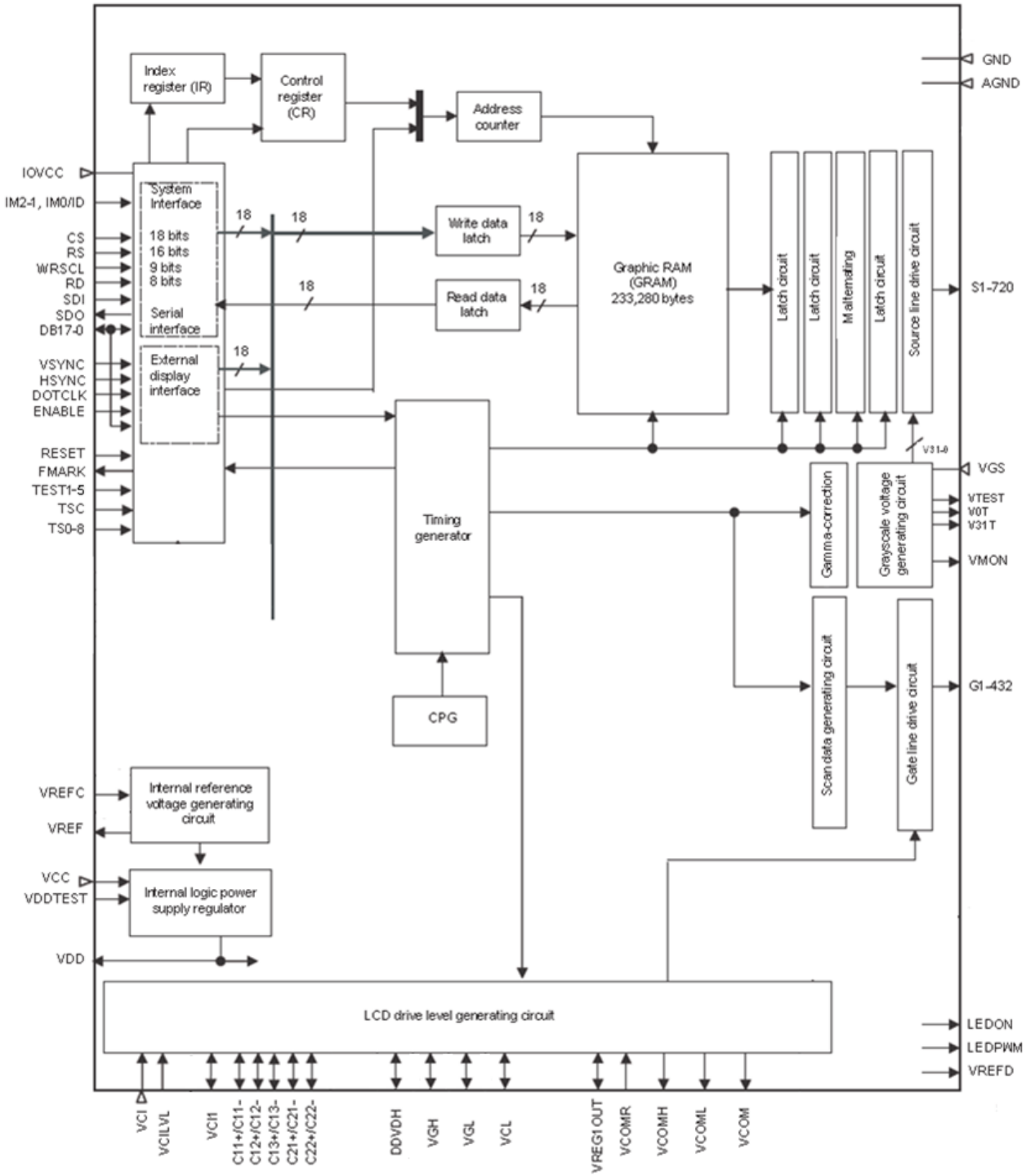
    Note : The Value given above is under Vci=2.5V
  - Built-in internal oscillator and hardware reset

3. ORDERING INFORMATION

Product Number	Package Type
OTM4001A-C	Chip Form with Gold Bump, thickness 400um
OTM4001A-C1	Chip Form with Gold Bump, thickness 280um

4. BLOCK DIAGRAM

4.1. Block Function



4.2. System Interface

4.2.1. The OTM4001A supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. Serial Peripheral Interface (SPI).

The OTM4001A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM4001A executes the 1st read operation. Thus, valid data can be read out after the OTM4001A executes the 1st read operation.

4.2.2. External Display Interface

The OTM4001A supports external RGB interface for picture movement display.

The OTM4001A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.2.3. Address Counter (AC)

OTM4001A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.2.4. Graphics RAM (GRAM)

OTM4001A features a 233,280-byte (240RGB x 432 x 18 / 8) Graphic RAM (GRAM).

4.2.5. Grayscale Voltage Generating Circuit

OTM4001A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.2.6. Timing Controller

OTM4001A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.2.7. Oscillator (OSC)

The OTM4001A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.2.8. Source Driver Circuit

OTM4001A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.2.9. Gate Driver Circuit

OTM4001A consists of a 432-output gate driver circuit (G1~G432). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VLOUT2, VLOUT3 and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

4.2.11. CABC Circuit

Backlight can be controlled by LEDPWM. Therefore, backlight level can be adjusted automatically depended on the display content to save power and maintain the same display quality.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="4">System Configuration Input Signal</td></tr>
<tr><td>IM2~1, IM0/ID</td><td>I</td><td>GND/ IOVCC</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td></tr>
<tr><td>/RESET</td><td>I</td><td>MPU or external RC circuit</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="4">Interface input Signals</td></tr>
<tr><td>/CS</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the OTM4001A is accessible
High: the OTM4001A is not accessible
Must be connected to the GND or IOVCC level when not used.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must be connected to the GND or IOVCC level when not used.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.</td></tr>
<tr><td>/RD</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must be connected to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Serial Data is inputted on the rising edge of the SCL signal in SPI mode.
Must be connected to the GND or IOVCC level when not in use</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Serial Data is outputted on the rising edge of the SCL signal in SPI mode.</td></tr>
<tr><td>DB0-DB17</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>6-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-13, DB11-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
</table>
Must be connected to the GND or IOVCC level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>In external interface mode, served as a vertical synchronize signal input</td></tr>
</table>

Signal	I/O	Connected with	Function
			Must be connected to the IOVCC or GND level when not in use.
HSYNC	I	MPU	In external interface mode, served as a horizontal synchronized signal input Must be connected to the IOVCC or GND level when not used.
ENABLE	I	MPU	In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 High: Invalid data on DB17-DB0 Moreover, setting EPL bit can change the polarity of the ENABLE signal. Must be connected to the GND or IOVCC level when not in use.
DOTCLK	I	MPU	In external interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK It is fixed to the IOVCC level when not in use.
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. Keep this pin open when not used.
CABC Signal			
LEDON	O	LED	Control pin for backlight on/off. Leave this pin open when not in use.
LEDPWM	O	LED	Pulse signal to control backlight level. Leave this pin open when not in use.
Charge Pump and Power Supply Signal			
C11P/N, C12P/N C13P/N C21P/N, C22P/N	I/O	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCI1	I/O	Stabilizing capacitor	Reference voltage of step-up circuit 1. VC bits set the output factor. To connect to stabilizing capacitor is need. Make sure the output voltage levels from VLOUT1, VLOUT2, and VLOUT3 do not exceed the respective setting ranges.
DDVDH	I/O	Stabilizing capacitor	Output voltage from the step-up circuit 1, generated from VCI1. Power supply for the source driver liquid crystal drive unit and VCOM drive. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. DDVDH = 4.5V ~ 6.0V
VGH	I/O	Stabilizing capacitor	Liquid crystal drive power supply.Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT2 = max 15.0V
VGL	I/O	Stabilizing capacitor	Liquid crystal drive power supply.Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT3 = min –12.5V
VCL	I/O	Stabilizing capacitor	VCOML drive power supply.Output voltage from the step-up circuit 2, generated from VCI1. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT = -1.9V – 3.0V.
VCILVL	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.6V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
Source/Gate Driver and VCOM Signals			
G1~G432	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltages are outputted.
VREG1 OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	O	Stabilizing	The High level of VCOM amplitude. The output level can be adjusted by either external

Signal	I/O	Connected with	Function
		capacitor	resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5)V ~ 0V. Make sure to connect to stabilizing capacitor.
VCOMR	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.
VGS	I	GND	Reference level for the grayscale voltage generating circuit.
VCC	-	Power supply	Internal logic power: VCC = 2.5V ~3.6V. VCC > IOVCC.
GND	-	Power supply	Internal logic GND: GND = 0V.
VDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. VCC ≥IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.6V.
Misc. Signal			
VTEST	I/O	Open	Test pins. Leave them open. OTM4001A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VREFC	I/O	AGND	Test pins. Fix to the AGND level.
VREF	I/O	Open	Test pins. Leave them open.
PROTECT	I/O	Open	Test pins. Leave them open.
VDDTEST	I/O	AGND	Test pins. Fix to the AGND level.
VREFD	I/O	Open	Test pins. Leave them open. OTM4001A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VMON	I/O	Open	Test pins. Leave them open. OTM4001A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VCIR	I/O	Open	Test pins. Leave them open. OTM4001A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
TSC	I/O	GND	Test pins. Fix to the GND level.
IOVCCDUM1~2	I/O	Open	Test pins. Leave them open.
VCCDUM1	I/O	Open	Test pins. Leave them open.
AGNDDUM1~5	I/O	AGND	Test pins. Fix to the AGND level.
DUMMYR1~4	I/O	Open	Test pins. Leave them open. OTM4001A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
DUMMYX	I/O	Open	Test pins. Leave them open.
DUMMYY	I/O	Open	Test pins. Leave them open.
DUMMYZ	I/O	Open	Test pins. Leave them open.
DUMMYA	I/O	Open	Test pins. Leave them open.
DUMMYC	I/O	Open	Test pins. Leave them open.
GNDDUM1~10	I/O	Open	Test pins. Leave them open.
VGLDMY1~4	I/O	Open	Test pins. Leave them open.
TESTO1~15	I/O	Open	Test pins. Leave them open.
TS0~8	I	Open	Test pins. Leave them open.
TEST1~5	I	GND	Test pins. Connect to GND level.

6. INSTRUCTIONS

6.1. Outline

The OTM4001A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for OTM4001A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in **Figure 6-1** to **Figure 6-6**

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

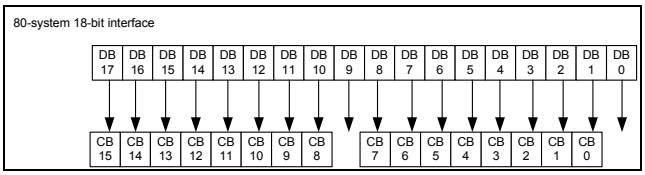


Figure 6-1

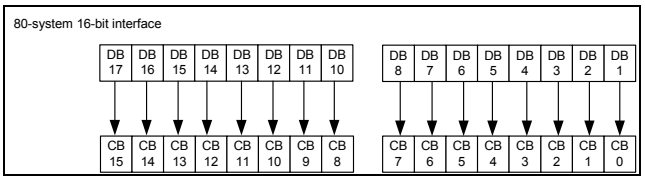


Figure 6-2

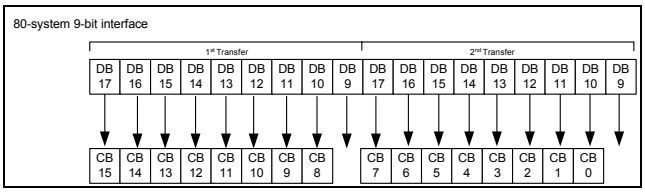


Figure 6-3

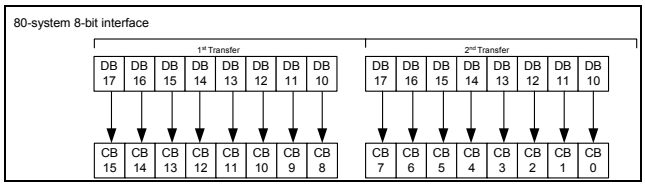


Figure 6-4

Serial interface Data Format

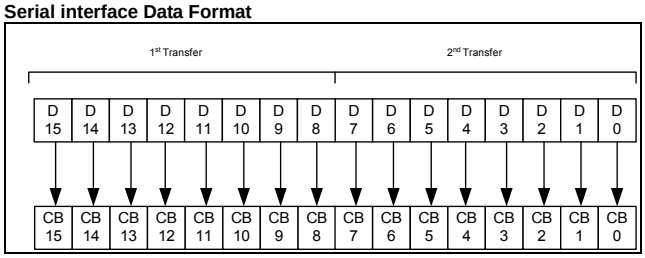


Figure 6-5

Serial interface Data Transfer Format

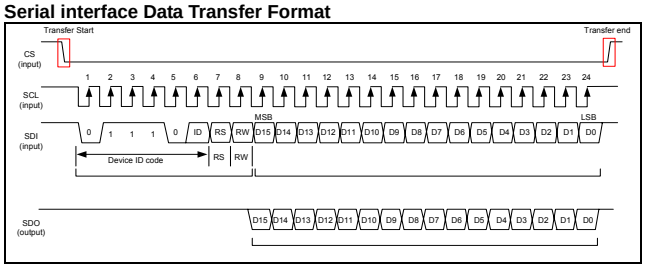


Figure 6-6

6.2. Instruction

Table 6-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
000h	ID Read	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0
001h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
002h	LCD Drive Waveform Control	0	0	0	0	0	0	0	B/C (0)	0	0	0	0	0	0	0	0
003h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)
004h-006h	Setting disabled																
007h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)
008h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
009h	Low Power Control (1)	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
00Ah	Setting Disabled																
00Bh	Low Power Control (2)	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)
0Ch	External Display Controll (1)	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
00Dh-00Eh	Setting Disabled																
00Fh	External Display Controll (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
010h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)
011h	Panel interface Control 2	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)
012h	Panel interface Control 3	0	0	0	0	0	0	VEQW11 (0)	VEQW10 (0)	0	0	0	0	0	0	0	0
013-01Fh	Setting Disabled																
020h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
021h	Panel Interface Control 5	0	0	0	0	NOWE3 (0)	NOWE2 (0)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	SDTE3 (0)	SDTE2 (0)	SDTE1 (0)	SDTE0 (0)
022h	Panel Interface Control 6	0	0	0	0	0	VEQWE2 (0)	VEQWE1 (0)	VEQWE0 (0)	0	0	0	0	0	0	0	0
023h-050h	Setting Disabled																
051h	WRDISBV	0	0	0	0	0	0	0	0	DBV7 (0)	DBV6 (0)	DBV5 (0)	DBV4 (0)	DBV3 (0)	DBV2 (0)	DBV1 (0)	DBV0 (0)
052h	RDDISBV	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
053h	WRCTRLD	0	0	0	0	0	0	0	0	BC_OUT _INV (0)	LED_ON (0)	BCTRL (0)	0	DD (0)	BL (0)	0	0
054h	RDCTRLD	0	0	0	0	0	0	0	0	BC_OUT _INV	LED_ON	BCTRL	0	DD	BL	0	0
055h	WRCABC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1 (0)	C0 (0)
056h	RDCABC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0
05Eh	WRCABCMB	0	0	0	0	0	0	0	0	CMB7 (0)	CMB6 (0)	CMB5 (0)	CMB4 (0)	CMB3 (0)	CMB2 (0)	CMB1 (0)	CMB0 (0)
05Fh	RDCABCMB	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0
090h	Frame Marker Control	FMKM (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
091h-0FFh	Setting disabled																
100h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
101h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
102h	Power Control (3)	0	0	0	0	0	0	0	VCMR0 (0)	VREG1R (0)	0	0	0	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
103h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
104h-106h	Setting disabled																
107h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
108-10Fh	Setting disabled																
110h	Power Control(6)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
111-1ffh	Setting disabled																
200h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
201h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
202h	Write Data to GRAM Read Data from GRAM	Data format is varied according to “interface”.															
203-20Fh	Setting disabled																
210h	Window Horzontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)

211h	Window Horzontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
212h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
213h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
214-280h	Setting Disabled																
281h	VCom high voltage 1	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
282h	VCom high voltage 2	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
283-2FFh	Setting disabled																
300h	γ Control (1)	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
301h	γ Control (2)	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
302h	γ Control (3)	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
303h	γ Control (4)	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
304h	γ Control (5)	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
305h	γ Control (6)	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
306h	γ Control (7)	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
307h	γ Control (8)	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
308h	γ Control (9)	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0
309h	γ Control (10)	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
30Ah	γ Control (11)	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
30Bh	γ Control (12)	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
30Ch	γ Control (13)	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
30Dh	γ Control (14)	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
30Eh	γ Control (15)	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
30Fh	γ Control (16)	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0
310-3FFh	Setting disabled																
400h	Size of base image	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
401h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
402-403h	Setting disabled																
404h	Vertical Scoll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
405-4FFh	Setting disabled																
500h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
501h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
502h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
503h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)
504h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
505h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
506-5FF	Setting Disabled																
600h	Software reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRFT
601h	CABC RAM Bank Sel	0	0	0	0	0	0	0	0	0	0	0	0	0	Bank2	Bank1	Bank0
602h	CABC RAM Write	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
603h	CABC RAM Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
606h	i80-I/F Endian Control	0	0	0	0	0	0	0	TCREV1 (0)	0	0	0	0	0	0	0	TCREV0 (0)
607-FFFh	Setting disabled																

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6.2.1. Index Register (IR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	0	0	0	0	0	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R000h ~ RFFFh) of a control register.

6.2.2. ID Read Register (R000h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0

The IC code of OTM4001A can be accessed by read operation. ‘5420H’ can be read out when read ID operation is exectued.

6.2.3. Driver Output Control Register (R001h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM(0)	0	SS(0)	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = “0”, source driver shifts from S1 to S720. When SS = “1”, source driver shifts from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-2.**

Table 6-2

SS=0;BGR=0;	S1	S2	S3	····▶	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	····▶	S718	S719	S720
SS=1,BGR=0;	S1	S2	S3	◀····	S718	S719	S720
SS=1,BGR=1;	S1	S2	S3	◀····	S718	S719	S720

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-3**.

Table 6-3

SM	GS	Shift Direction (begin,…..,end)
0	0	G1, G2, G3, G4……G429, G430, G431, G432
0	1	G432, G431, G430, G429……G4, G3, G2, G1

6.2.4. LCD Driving Waveform Control (R002h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	B/C(0)	0	0	0	0	0	0	0	0

B/C: This bit .is to set the Vcom toggle at frame rate format of N-line inversion format.

B/C=0: Frame inversion.

B/C=1: 1-line inversion.

6.2.5. Entry Mode (R003h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI REG(0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)

Table 6-4

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

AM: To set the update direction when writing data to GRAM. If AM=1, data will write in vertical direction. If AM=0, data will write in horizontal direction. Moreover, if a fixed window GRAM accessing is desired, the writing direction can be set by I/D1-0 and AM bits.

I/D1-0: To specify address counter increment / decrement automatically function while GRAM is accessing. I/D[0] indicates the increment or decrement in horizontal direction. I/D[1] indicates the increment or decrement in vertical direction.

I/D[0]=0: decrement in horizontal direction automatically

I/D[0]=1: increment in horizontal direction automatically

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with AM bit to set the data updating direction.

ORG: OTM4001A provides the option of start address definition when window function is selected.

ORG=1: RAM address setting should set to (00000h) no matter where the window start address is. In this case, the window start postion is treated as (00000h), regardless the physical location in GRAM.

ORG=0: RAM address setting should set to the address.

BGR: To set the order of RGB dot location in GRAM.

BGR=0: same assignment of RGB allocation of DB17-0

BGR=1: inverse assignment of RGB allocation of DB17-0

DFM: In combination with TRIREG setting to set the different data transfer mode.

TRIREG: to set 1–3 time transfer mode for system interface. TRIREG bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit databus interface mode:

TRIREG=0: 2 time transfer mode for 16-bit GRAM data.

TRIREG=1: 3 time transfer mode for 18-bit GRAM data

For 16-bit databus interface mode:

TRIREG=0: 1 time transfer mode for 16-bit GRAM data.

TRIREG=1: 2 time transfer mode for 18-bit GRAM data

Note: Set TRIREG=0, when using neither 8-bit nor 16-bit.

EPF1-0: To select the algorithm of expanding 8/16 bits to 18 bits. This setting is valid only when 16-bit or 8-bit interfaces are in use.

6.2.6. Display Control 1 (R007h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; OTM4001A is set to standby mode. The combination of D1-0 and BASEE bit is summarized at **Table 6-5**.

Table 6-5

D1	D0	BASEE	Source, VCOM output	Internal Operation	FLM
0	0	*	GND	Terminated	OFF
0	1	*	GND	Normal Operation	ON
1	0	*	Non-lit display	Normal Operation	ON
1	1	0	Non-lit display	Normal Operation	ON
		1	Normal display	Normal Operation	ON

DTE, GON: Specify the high/low level of gate driver output signal. The combination of DTE and GON bit is summarized at **Table 6-6**.

Table 6-6

APE	GON	DTE	Gate Output
0	*	*	VGL(=GND)
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	1	VGH/VGL

Table 6-7

APE	AP [2:0]	VCOMG	VCOM Output
0	*	*	GND
1	000	0	GND
	000	0-1	Setting Disabled
	000	1	Setting Disabled
	001-111	0	GND
	001-111	1	VCOML
	001-111	0	VCOMH/GND
	001-111	1	VCOMH/VCOML

BASEE: To enable Base image display

BASEE	
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

PTDE1-0: To set the partial-display enables function.

PTDE [0]: "0" Partial image 1 display "Off".
"1" Partial image 1 display "On".

PTDE [1]: "0" Partial image 2 display "Off".
"1" Partial image 2 display "On".

6.2.7. Display Control 2 (R008h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 6-8 summarized the function of FP3-0/BP3-0 setting. When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-9** summarized the setting for each interface mode.

Table 6-8

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

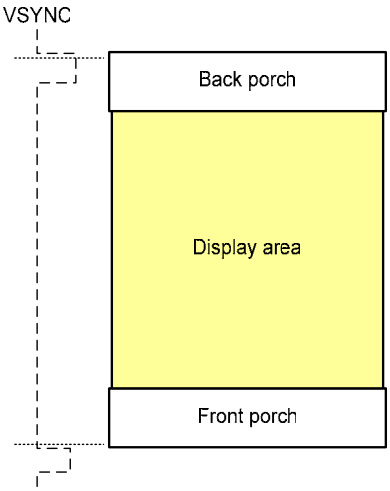


Figure 6-7 Front porch and back porch function diagram

Table 6-9

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

6.2.8. Display Control 3 (R009h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)

ISC3-0: To set the gate driver scan cycle in non-display area. **Table 6-10** summarized the function of ISC3-0 setting

Table 6-10

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	Setting disable	
0	0	0	1	3frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1000-1111				Setting Disabled	

PTG1-0: To set the gate driver scan mode in non-display area. **Table 6-11** summarized the function of PTG1-0 setting

Table 6-11

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Setting Disable		
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Setting Disable		

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 6-12** summarized the function of PTS2-0 setting.

Table 6-12

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area
			+ve polarity	-ve polarity	
0	0	0	V31	V0	V0-V31
001-011			Setting inhibited		
1	0	0	V31	V0	V0-V31
101-111			Setting inhibited		

PTV: To set VCOM output in non-display area, Vcom operates normally when PTV = 1, and stops operation when PTV = 0.

6.2.9. Low Power Control (R00Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)

COL:

COL = 0: 262,144 colors

COL = 1: 8 colors.

In 8-color mode, the source output is either connected to VREGIOUT or GND.

VEM0: VEM0 = 1, when VCOM is switched from VCOMH to VCOML, it will dropped to GND level in the intermediate stage.

VEM0 = 0, when VCOM is switched from VCOMH to VCOML, it will directly change to VCOML level.

6.2.10. External Display Interface Control 1 (R00Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)

RIM1-0: To set the different transfer modes of RGB interface.

Table 6-13 summarized the function of RIM1-0 setting.

Table 6-13

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12
1	1	Setting disabled	-	-

DM1-0: To specify the display interface mode.

Table 6-14summarized the function of DM1-0 setting.

Table 6-14

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the OTM4001A's internal GRAM. The setting of RM should be consistent with DM1-0. **Table 6-15** summarized the function of RM bit setting.

Table 6-15

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

6.2.11. External Display Interface Control 2 (R00Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.
DPL = ”0”: rising edge of the DOTCLK.
DPL =”1”: falling edge of the DOTCLK.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.
HSPL = ”0”: Low active.
HSPL = ”1”: High active.

EPL: The polarity of ENABLE signal selection in RGB interface mode.
EPL = “0”: ENABLE: Low active
EPL = ”1”: ENABLE: High active

VSPL: The polarity of VSYNC signal selection in RGB interface mode.
VSPL = ”0”: Low active.
VSPL = ”1”: High active.

6.2.12. Panel Interface Control 1 (R010h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)

RTNI4-0: Set the clock cycle per line **Table 6-16** summarized the function of RTNI4-0 setting.

Table 6-16

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIVI1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIVI bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVI1-0 bits are disabled. **Table 6-17** summarized the function of DIVI1-0 setting.

Table 6-17

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIVI bits

Clock cycles per line: RTNI bits

FP: the number of lines for the front porch period

BP: the number of lines for the back porch period

6.2.13. Panel Interface Control 2 (R011h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 6-18** summarized the function of NOWI2-0 setting.

Table 6-18

NOWI2	NOWI1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

SDTI2-0: Set the delay of source output in every line.

Table 6-19

SDTI2	SDTI1	SDTI0	Source output delay period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.14. Panel Interface control 3 (R012h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	VEQW1 (0)	VEQW0 (0)	0	0	0	0	0	0	0	0	0

VEQWI[1:0]: Set VCOM equalize period.

Table 6-20

VEQWI1	VEQWI0	VCOM Equalize Period
0	0	0 clock
0	1	1 clock
1	0	2 clocks
1	1	3 clocks

6.2.15. Panel Interface control 4 (R020h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)

RTNE6-0: Set the clock cycle per line **Table 6-21** summarized the function of RTNE5-0 setting.

Table 6-21

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
0	0	0	0	0	0	Setting disable
Setting disable						
0	1	0	0	0	0	16 clocks
0	1	0	0	0	1	17 clocks
0	1	0	0	1	0	18 clocks
0	1	0	0	1	1	19 clocks
0	1	0	1	0	0	20 clocks
0	1	0	1	0	1	21 clocks
0	1	0	1	1	0	22 clocks
0	1	0	1	1	1	23 clocks
0	1	1	0	0	0	24 clocks
0	1	1	0	0	1	25 clocks
0	1	1	0	1	0	26 clocks
0	1	1	0	1	1	27 clocks
0	1	1	1	0	0	28 clocks
0	1	1	1	0	1	29 clocks
0	1	1	1	1	0	30 clocks
0	1	1	1	1	1	31 clocks
1	0	0	0	0	0	32 clocks
1	0	0	0	0	1	33 clocks
1	0	0	0	1	0	34 clocks

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
1	0	0	0	1	1	35 clocks
1	0	0	1	0	0	36 clocks
1	0	0	1	0	1	37 clocks
1	0	0	1	1	0	38 clocks
1	0	0	1	1	1	39 clocks
1	0	1	0	0	0	40 clocks
1	0	1	0	0	1	41 clocks
1	0	1	0	1	0	42 clocks
1	0	1	0	1	1	43 clocks
1	0	1	1	0	0	44 clocks
1	0	1	1	0	1	45 clocks
1	0	1	1	1	0	46 clocks
1	0	1	1	1	1	47 clocks
1	1	0	0	0	0	48 clocks
1	1	0	0	0	1	49 clocks
1	1	0	0	1	0	50 clocks
1	1	0	0	1	1	51 clocks
1	1	0	1	0	0	52 clocks
1	1	0	1	0	1	53 clocks
1	1	0	1	1	0	54 clocks
1	1	0	1	1	1	55 clocks
1	1	1	0	0	0	56 clocks
1	1	1	0	0	1	57 clocks
1	1	1	0	1	0	58 clocks
1	1	1	0	1	1	59 clocks
1	1	1	1	0	0	60 clocks
1	1	1	1	0	1	61 clocks
1	1	1	1	1	0	62 clocks
1	1	1	1	1	1	63 clocks

DIVE1-0: To specified the division ratio of internal operation clock frequency. Set the RTNE and DIVE bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVE1-0 bits are disabled. **Table 6-22** summarized the function of DIVE1-0 setting.

Table 6-22

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency (16 bit, one time transfer)	Internal Operation Clock Frequency (8 bit, three time transfer)
0	0	Setting disable		
0	1	4	fosc / 4	fosc / 12
1	0	8	fosc / 8	fosc / 24
1	1	16	fosc / 16	fosc / 48

fosc =Frequency of RC oscillation

6.2.16. Panel Interface Control 5 (021Rh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOWE3(0)	NOWE2(0)	NOWE1(0)	NOWE0(0)	0	0	0	0	SDTE3(0)	SDTE2(0)	SDTE1(0)	SDTE0(0)

NOWE [3:0]: Set the adjacent gate driver output non-overlap period in RGB interface. **Table 6-23** summarized the function of NOWE3-0 setting.

SDTE: Set the source output delay in RGB interface.

Table 6-23

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

Table 6-24

SDTE3	SDTE 2	SDTE 1	SDTE 0	Source output period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

6.2.17. Panel Interface Control 6 (R022h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	VEQ WE2(0)	VEQ WE1(0)	VEQ WE0(0)	0	0	0	0	0	0	0	0

VEQWE2-0: To set the drive period of low power VCOM, which is valid when the operation is synchronized with RGB interface signals.

Table 6-25

VEQWE2	VEQWE1	VEQWE0	Source Output Delay Perios
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.18. CABC Write Display Brightness (R051h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to adjust the brightness value of the display.

It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

6.2.19. CABC Read Display Brightness (R052h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

6.2.20. CABC Write Control Display (R053h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	BC_OUT_INV	LED_ON	BCTRL	0	DD	BL	0	0

This command is used to control brightness and gamma settings.
BCTRL : Brightness control block on/off, This bit is always used to switch brightness for display.
0 = off (brightness registers are 00h)
1 = on (brightness registers are active)

DD : Display dimming
0 = Display dimming is off.
1 = Display dimming is on.

BL : Backlight control on/off
0 = off (completely turn off backlight circuit)
1 = on

LEDON : Backlight LED control signal.
0 = off
1 = on

BC_OUT_INV : Inverse the polarity of LEDPWM signal
0 = no inversion
1 = inversion

6.2.21. CABC Read Control Display (R054h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	BC_OUT_INV	LED_ON	BCTRL	0	DD	BL	0	0

This command is used to read control brightness and gamma settings back.
BCTRL : Brightness control block on/off, This bit is always used to switch brightness for display.
0 = off (brightness registers are 00h)
1 = on (brightness registers are active)

DD : Display dimming
0 = Display dimming is off.
1 = Display dimming is on.

BL : Backlight control on/off
0 = off (completely turn off backlight circuit)
1 = on

LEDON : Backlight LED control signal.
0 = off
1 = on

BC_OUT_INV : Inverse the polarity of LEDPWM signal
0 = no inversion
1 = inversion

6.2.22. Write Content Adaptive Brightness Control (R055h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

This command is used to set parameters for image content based adaptive brightness control functionality.

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

6.2.23. Read Content Adaptive Brightness Control (R056h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

This command is used to read parameters for image content based adaptive brightness control functionality back.

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

6.2.24. Write CABC minimum brightness (R05Eh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

This command is used to set the minimum brightness value of the display for CABC function.
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the hight brightness for CABC.

6.2.25. Read CABC minimum brightness (R05Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

This command returns the minimum brightness value of CABC function.
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the hight brightness for CABC.

6.2.26. Frame Marker Control (R090h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	FMKM (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)

FMP8-0: Set the position of the frame marker. 0 ≤ FMP ≤ BP + NL + FP

Table 6-26

FMP8-0	Frame Marker Position
000000000	0
000000001	1
000000010	2
000000011	3
…	…
110111100	444
110111101	445
110111110	446
110111111	447

FMI2-0: Set the period of the Frame Marker.

Table 6-27

FMI2	FMI1	FMI0	Period of FMARK
0	0	0	1 frame
0	1	1	2 frames
1	0	1	4 frames
1	1	1	6 frames

FMKM:

0: Disable FMARK

1. Enable FMARK

6.2.27. Power Control 1 (R100h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	AP2 (1)	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0

SLP: Sleep mode selection. When SLP =1, OTM4001A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to "1". In sleep mode, no instruction can be accepted. Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are remained unchanged.

DSTB: Deep Standby mode selection. When DSTB =1, OTM4001A set to deep standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set DSTB to "1". Set DSTB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set DSTB to "0". Moreover, when exit from deep standby mode, data in GRAM and register would be lost, reset and re-sending command and data into GRAM are necessary.

AP2-0: Operational amplifier DC bias current adjustment. Set AP2-0 = "000" to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during non display period. **Table 6-28** summarized the function of AP2-0 setting. Please note that the values listed in the table are the ratios of the currents of the corresponding settings to the current at the max rank.

Table 6-28

AP2	AP1	AP0	Constant current in power supply circuit	Constant current in Gamma circuit
0	0	0	Halt	Halt
0	0	1	0.5	0.5
0	1	0	0.6	0.6
0	1	1	0.8	0.8
1	0	0	1	1
1	0	1	1.2	1.2
1	1	0	1.4	1.4
1	1	1	1.9	1.9

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE="0", Halt liquid crystal power supply and gamma voltage generation circuit

APE="1", Enable liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and VCL.

Table 6-29 summarized the function of BT2-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL	Capacitor connection pins
0	0	0	VCI1 x 2 [VCI1x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1 [VCI1x-1]	
0	0	1	VCI1 x 2 [VCI1x2]	DDVDH x 3 [VCI1 x 6]	-(DDVDHx 2) [VCI1x -4]	-VCI1 [VCI1x-1]	
0	1	0	VCI1 x 2 [VCI1x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1 [VCI1x-1]	
0	1	1	VCI1 x 2 [x2]	DDVDH x 3 - VCI1 [VCI1 x 5]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1 [VCI1x-1]	
1	0	0	VCI1 x 2 [x2]	DDVDH x 3 - VCI1 [VCI1 x 5]	-(DDVDHx 2) [VCI1x -4]	-VCI1 [VCI1x-1]	
1	0	1	VCI1 x 2 [x2]	DDVDH x 3 - VCI1 [VCI1 x 5]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1 [VCI1x-1]	
1	1	0	VCI1 x 2 [x2]	DDVDH x 2 [VCI1 x 4]	-(DDVDHx 2) [VCI1x -4]	-VCI1 [VCI1x-1]	
1	1	1	VCI1 x 2 [x2]	DDVDH x 2 [VCI1 x 4]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1 [VCI1x-1]	

SAP: Enable bit for gamma voltage generation circuit.

SAP="0", Halt gamma voltage generation circuit.

SAP="1", Enable gamma voltage generation circuit.

6.2.28. Power Control 2 (R101h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (0)	0	DC02 (1)	DC01 (1)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)

VC2-0: Set the voltage of VCI1. VCI1 is generated by VCILVL. **Table 6-30** summarized the function of VC2-0 setting

Table 6-30

VC2	VC1	VC0	VCI1
0	0	0	0.94 x VCILVL
0	0	1	0.89 x VCILVL
0	1	0	Setting Disable
0	1	1	Setting Disable
1	0	0	0.76 x VCILVL
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	1.00 x VCILVL

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 6-31** summarized the function of DC02-00 setting

Table 6-31

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	Oscillation clock
0	0	1	Oscillation clock / 2
0	1	0	Oscillation clock / 4
0	1	1	Oscillation clock / 8
1	0	0	Oscillation clock / 16
1	0	1	Invalid Setting
1	1	0	Invalid Setting
1	1	1	Invalid Setting

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 6-32** summarized the function of DC12-10 setting

Table 6-32

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 128
1	0	0	Oscillation clock / 256
1	0	1	Setting disabled
1	1	0	Setting disabled
1	1	1	Setting disabled

6.2.29. Power Control 3 (R102h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VCMR0(0)	VREG1R(0	0	0	0	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)

VRH3-0: Set the voltage level of VREG1OUT, which generated from VCILVL. **Table 6-33** summarized the function of VRH3-0 setting

Table 6-33

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage		VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCILVL	VCIR					VCILVL	VCIR
0	0	0	0	Halt	Halt	1	0	0	0	VCILVLx1.6	2.5Vx1.6
0	0	0	1	Halt	Halt	1	0	0	1	VCILVLx1.65	2.5Vx1.65
0	0	1	0	Halt	Halt	1	0	1	0	VCILVLx1.7	2.5Vx1.7
0	0	1	1	Halt	Halt	1	0	1	1	VCILVLx1.75	2.5Vx1.75
0	1	0	0	Setting disable	Setting disable	1	1	0	0	VCILVLx1.8	2.5Vx1.8
0	1	0	1	Setting disable	Setting disable	1	1	0	1	VCILVLx1.85	2.5Vx1.85
0	1	1	0	Setting disable	Setting disable	1	1	1	0	VCILVLx1.9	2.5Vx1.9
0	1	1	1	Setting disable	Setting disable	1	1	1	1	Setting disable	Setting disable

VREG1R: Select reference voltage for VREG1OUT

VREG1R = “0” (default): VCILVL (External) as reference voltage for VREG1OUT.

VREG1R = ”1”: VCIR (internal) as reference voltage for VREG1OUT.

VCMR[0]: Select VCOMH external resistance or internal setting for VCOMH voltage level.

VCMR[0] = “0” use VCOMR (External) setting as VCOMH voltage.

VCMR[0] = ”1”: use register (Internal) setting as VCOMH voltage.

6.2.30. Power Control 4 (R103h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated from VREG1OUT, the coefficient is valid from 0.7 to 1.24.

Table 6-34

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 1.02
1	0	0	0	1	VREG1OUT x 1.04
1	0	0	1	0	VREG1OUT x 1.06
1	0	0	1	1	VREG1OUT x 1.08
1	0	1	0	0	VREG1OUT x 1.10
1	0	1	0	1	VREG1OUT x 1.12
1	0	1	1	0	VREG1OUT x 1.14
1	0	1	1	1	VREG1OUT x 1.16
1	1	0	0	0	VREG1OUT x 1.18
1	1	0	0	1	VREG1OUT x 1.20
1	1	0	1	0	VREG1OUT x 1.22
1	1	0	1	1	VREG1OUT x 1.24
1	1	1	0	0	Setting Disabled
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

6.2.31. GRAM Address Set (Horizontal Address) (R200h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

See R201h.

6.2.32. GRAM Address Set (Vertical Address) (R201h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the OTM4001A is in standby mode.

Table 6-35 summarized the function of AD15-0 setting

Note1: The address AD16-0 should be set in the address counter every frame on the falling edge of VSYNC if RGB interface mode is selected.

Note2: The address AD16-0 should be set when executing an instruction if system or VSYNC interface mode is selected.

Table 6-35

AD16–AD0	GRAM Setting
“00000”H – “000EF”H	Bitmap data for G1
“00100”H – “001EF”H	Bitmap data for G2
“00200”H – “002EF”H	Bitmap data for G3
“00300”H – “003EF”H	Bitmap data for G4
:	:
“1AC00”H – “1ACEF”H	Bitmap data for G399
“1AD00”H – “1ADEF”H	Bitmap data for G430
“1AE00”H – “1AEEF”H	Bitmap data for G431
“1AF00”H – “1AFEF”H	Bitmap data for G432

6.2.33. Write Data to GRAM (R202h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different transferring modes.															

WD17-0: OTM4001A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, OTM4001A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 6-36** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 6-8 ~ Figure 6-18** illustrates the pin assignment among data bus (DB17-0), (WD17-0) and GRAM.

Table 6-36

Data in GRAM	Source Driver Grayscale Output – REV=1 (REV=0)	
RGB	**Negative(Postive)**	**Positive(Negative)**
000000	V31	V0
000001	(V30+V31)/2	(V1+V0)/2
000010	V30	V1
000011	(V29+V30)/2	(V2+V1)/2
000100	V29	V2
000101	(V29+V28)/2	(V3+V2)/2
000110	V28	V3
000111	(V28+V27)/2	(V4+V3)/2
001000	V27	V4
001001	(V27+V26)/2	(V5+V4)/2
001010	V26	V5
001011	(V26+V25)/2	(V6+V5)/2
001100	V25	V6
001101	(V25+V24)/2	(V7+V6)/2
001110	V24	V7
001111	(V24+V23)/2	(V8+V7)/2
010000	V23	V8
010001	(V23+V22)/2	(V9+V8)/2
010010	V22	V9
010011	(V22+V21)/2	(V10+V9)/2
010100	V21	V10
010101	(V21+V20)/2	(V11+V10)/2
010110	V20	V11
010111	(V20+V19)/2	(V12+V11)/2
011000	V19	V12
011001	(V19+V18)/2	(V12+V11)/2
011010	V18	V13
011011	(V18+V17)/2	(V13+V12)/2
011100	V17	V14
011101	(V17+V16)/2	(V14+V13)/2
011110	V16	V15
011111	(V16+V15)/2	(V16+V15)/2
100000	V15	V16
100001	(V15+V14)/2	(V17+V16)/2
100010	V14	V17
100011	(V14+V13)/2	(V18+V17)/2
100100	V13	V18
100101	(V13+V12)/2	(V19+V18)/2
100110	V12	V19
100111	(V12+V11)/2	(V20+V19)/2
101000	V11	V20
101001	(V11+V10)/2	(V21+V20)/2
101010	V10	V21
101011	(V10+V9)/2	(V22+V21)/2
101100	V9	V22
101101	(V9+V8)/2	(V23+V22)/2
101110	V8	V23
101111	(V8+V7)/2	(V24+V23)/2
110000	V7	V24
110001	(V7+V6)/2	(V25+V24)/2
110010	V6	V25
110011	(V6+V5)/2	(V26+V25)/2
110100	V5	V26
110101	(V5+V4)/2	(V27+V26)/2
110110	V4	V27
110111	(V4+V3)/2	(V28+V27)/2
111000	V3	V28
111001	(V3+V2)/2	(V29+V28)/2
111010	V2	V29
111011	(V2+V1)/2	(V29+V30)/2
111100	V1	V30
111101	(V1+V0)/2	(V30+V31)/2
111110	(V1+2V0)/2	(V30+2V31)/2
111111	V0	V31

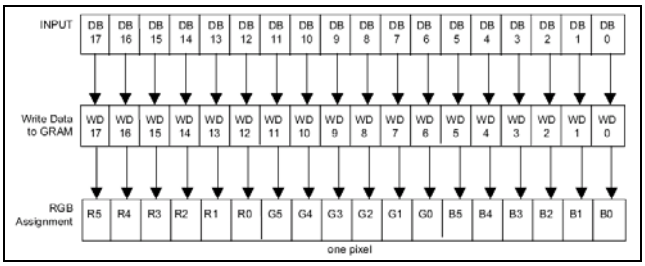


Figure 6-8 18-bit interface (262,144 colors)

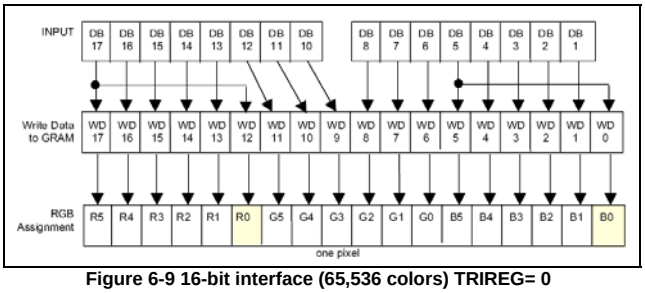


Figure 6-9 16-bit interface (65,536 colors) TRIREG= 0

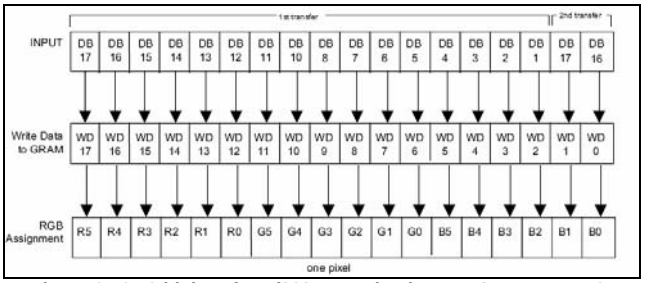


Figure 6-10 16-bit interface (262,144 colors) TRIREG = 1, DFM = 0

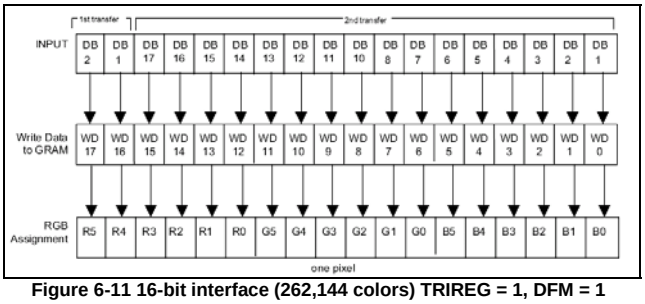


Figure 6-11 16-bit interface (262,144 colors) TRIREG = 1, DFM = 1

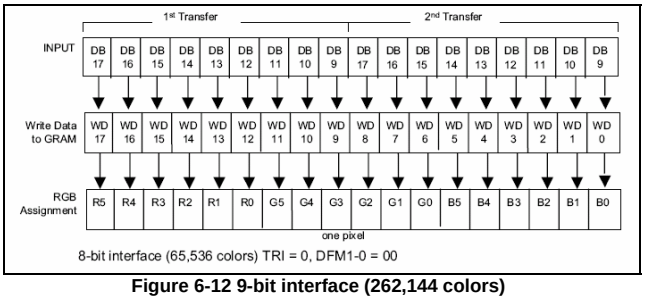


Figure 6-12 9-bit interface (262,144 colors)

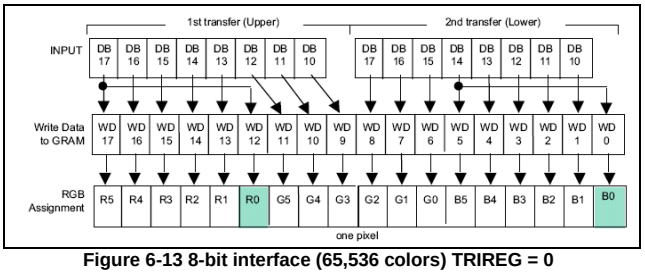


Figure 6-13 8-bit interface (65,536 colors) TRIREG = 0

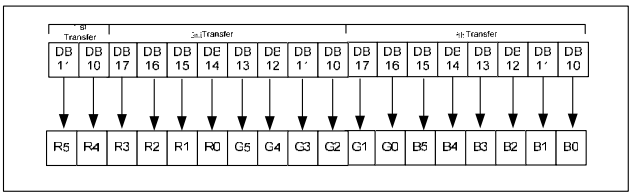


Figure 6-14 8-bit interface 262 colors) TRIREG = 1, DFM=0.

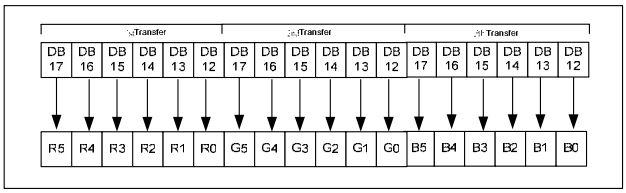


Figure 6-15 8-bit interface (262K colors) TRIREG = 1, DFM=1

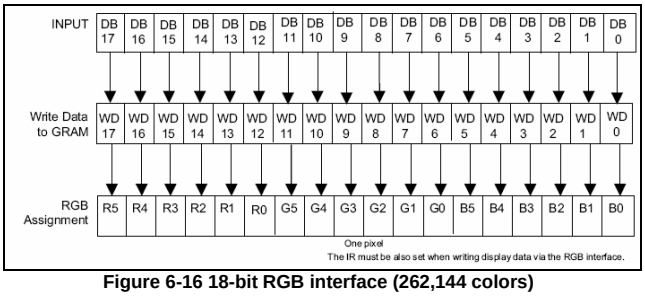


Figure 6-16 18-bit RGB interface (262,144 colors)

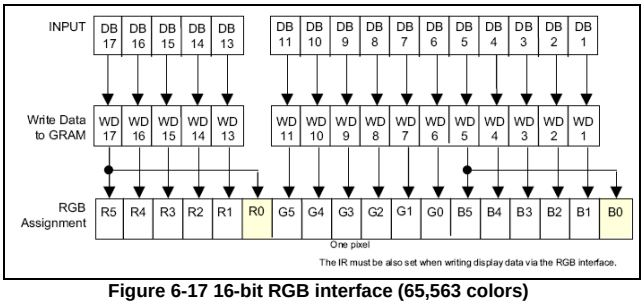


Figure 6-17 16-bit RGB interface (65,563 colors)

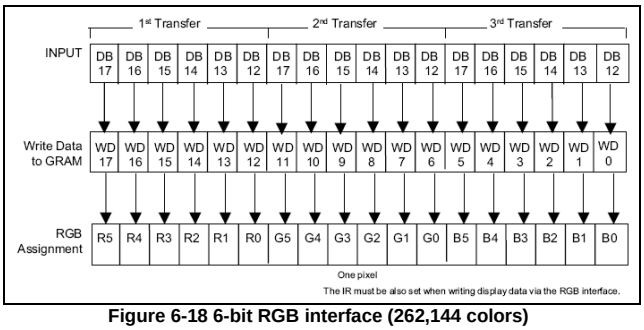


Figure 6-18 6-bit RGB interface (262,144 colors)

OTM4001A supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, OTM4001A also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = "Low". Set ENABLE "High" to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 6-19** illustrates the timing diagram while RGB and system interface are both use in the same time.

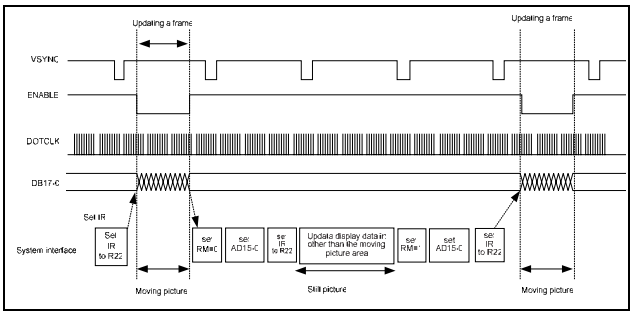


Figure 6-19

6.2.34. Read Data Read from GRAM (R202h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different transferring modes.															

R202 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note: This register is not available with the RGB interface. **Figure 6-20** and
Figure 6-23 **Figure 6-23** illustrates the pin assignment among data bus (DB17-0), R22 (RD17-0) and GRAM in read data instruction.

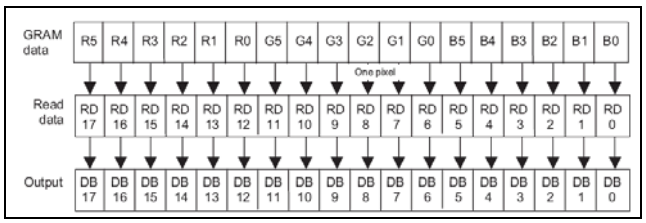


Figure 6-20 18-bit interface

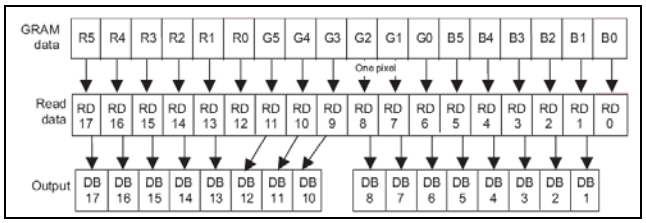


Figure 6-21 16-bit interface

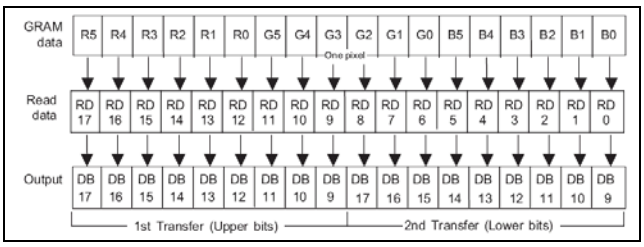


Figure 6-22 9-bit interface

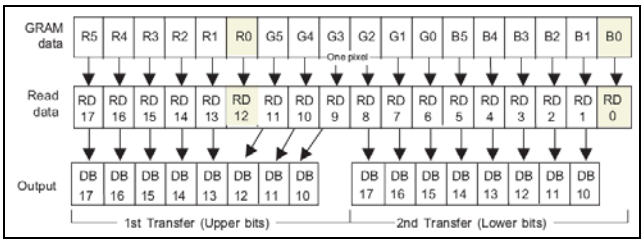


Figure 6-23 8-bit interface / SPI

6.2.35. NVM read data 2 (R281h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 14(0)	VCM 13(0)	VCM 12(0)	VCM 11(0)	VCM 10(0)

See R282h

6.2.36. NVM read data 3 (R282h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCM SEL	0	0	VCM 24(0)	VCM 23(0)	VCM 22(0)	VCM 21(0)	VCM 20(0)

VCM1 [4:0]: These pins are to set the factor for generating VCOMH when VCMSEL=”0”. **Table 6-37** summarized the the factor of VERG1OUT

VCM2 [4:0]: These pins are to set the factor for generating VCOMH when VCMSEL=”1”. **Table 6-38** summarized the the factor of VERG1OUT

Table 6-37

VCM1[4:0]	VCOMH voltage
5’h00	VREG1OUT x 0.69
5’h01	VREG1OUT x 0.70
5’h02	VREG1OUT x 0.71
5’h03	VREG1OUT x 0.72
5’h04	VREG1OUT x 0.73
5’h05	VREG1OUT x 0.74
5’h06	VREG1OUT x 0.75
5’h07	VREG1OUT x 0.76
5’h08	VREG1OUT x 0.77
5’h09	VREG1OUT x 0.78
5’h0A	VREG1OUT x 0.79
5’h0B	VREG1OUT x 0.80
5’h0C	VREG1OUT x 0.81
5’h0D	VREG1OUT x 0.82
5’h0E	VREG1OUT x 0.83
5’h0F	VREG1OUT x 0.84
5’h10	VREG1OUT x 0.85
5’h11	VREG1OUT x 0.86
5’h12	VREG1OUT x 0.87
5’h13	VREG1OUT x 0.88
5’h14	VREG1OUT x 0.89
5’h15	VREG1OUT x 0.90
5’h16	VREG1OUT x 0.91
5’h17	VREG1OUT x 0.92
5’h18	VREG1OUT x 0.93
5’h19	VREG1OUT x 0.94
5’h1A	VREG1OUT x 0.95
5’h1B	VREG1OUT x 0.96
5’h1C	VREG1OUT x 0.97
5’h1D	VREG1OUT x 0.98
5’h1E	VREG1OUT x 0.99
5’h1F	VREG1OUT x 1.00

Table 6-38

VCM2[4:0]	VCOMH voltage
5’h00	VREG1OUT x 0.69
5’h01	VREG1OUT x 0.70
5’h02	VREG1OUT x 0.71
5’h03	VREG1OUT x 0.72
5’h04	VREG1OUT x 0.73
5’h05	VREG1OUT x 0.74
5’h06	VREG1OUT x 0.75
5’h07	VREG1OUT x 0.76
5’h08	VREG1OUT x 0.77
5’h09	VREG1OUT x 0.78
5’h0A	VREG1OUT x 0.79
5’h0B	VREG1OUT x 0.80
5’h0C	VREG1OUT x 0.81
5’h0D	VREG1OUT x 0.82
5’h0E	VREG1OUT x 0.83
5’h0F	VREG1OUT x 0.84
5’h10	VREG1OUT x 0.85
5’h11	VREG1OUT x 0.86
5’h12	VREG1OUT x 0.87
5’h13	VREG1OUT x 0.88
5’h14	VREG1OUT x 0.89
5’h15	VREG1OUT x 0.90
5’h16	VREG1OUT x 0.91
5’h17	VREG1OUT x 0.92
5’h18	VREG1OUT x 0.93
5’h19	VREG1OUT x 0.94
5’h1A	VREG1OUT x 0.95
5’h1B	VREG1OUT x 0.96
5’h1C	VREG1OUT x 0.97
5’h1D	VREG1OUT x 0.98
5’h1E	VREG1OUT x 0.99
5’h1F	VREG1OUT x 1.00

VCMSEL: VCMSEL is to select VCM1 or VCM2; When VCMSEL=”0”, VCM1 is selected while VCMSEL=”1”, VCM2 is selected.

6.2.37. Window Horizontal RAM Address Start (R210h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HAS (0)2	HSA1 (0)	HSA0 (0)

See R213h.

6.2.38. Window Horziontal RAM Address End (R211h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)

See R213h.

6.2.39. Window Vertical RAM Address Start (R212h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)

See R213h.

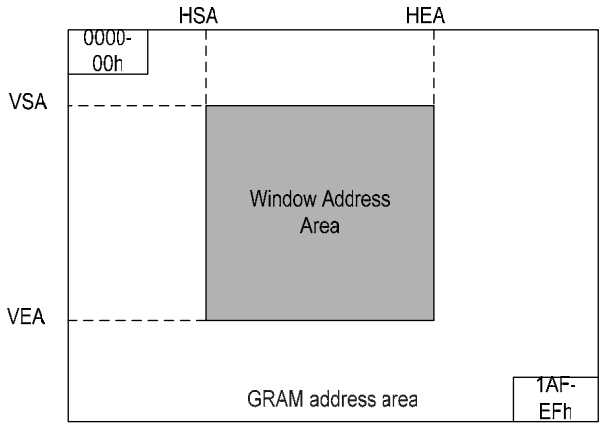
6.2.40. Window Vertical RAM Address End (R213h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (1)	VEA6 (1)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)

HSA7-0/HEA7-0: OTM4001A provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ HSA7-0< HEA7-0 ≤ “EF”h and HEA-HAS>=”04h”.

VSA8-0/VEA8-0: OTM4001A provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window-accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ VSA8-0< VEA8-0 ≤ 9’h1AF.

Figure 6-24 illustrates the window-accessing function.



6.2.41. γ Control (R300h to R30Fh)

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R300	W	1	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
R301	W	1	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
R302	W	1	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
R303	W	1	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
R304	W	1	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
R305	W	1	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
R306	W	1	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
R307	W	1	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
R308	W	1	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0
R309	W	1	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
R30A	W	1	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
R30B	W	1	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
R30C	W	1	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
R30D	W	1	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
R30E	W	1	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
R30F	W	1	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0

γ Control (R300h to R30Fh): OTM4001A provides 16 gamma registers to fine tune gamma output voltage.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment.
V7RP[4:0]: register for positive VSD13 fine tune adjustment.
V8RP[4:0]: register for positive VSD50 fine tune adjustment.
V9RP[3:0]: register for positive VSD4 fine tune adjustment.
V10RP[3:0]: register for positive VSD8 fine tune adjustment.
V11RP[3:0]: register for positive VSD20 fine tune adjustment.
V12RP[3:0]: register for positive VSD27 fine tune adjustment.
V13RP[3:0]: register for positive VSD36 fine tune adjustment.
V14RP[3:0]: register for positive VSD43 fine tune adjustment.
V15RP[3:0]: register for positive VSD55 fine tune adjustment.
V16RP[3:0]: register for positive VSD59 fine tune adjustment.

V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment.
V7RN[4:0]: register for negative VSD13 fine tune adjustment.
V8RN[4:0]: register for negative VSD50 fine tune adjustment.
V9RN[3:0]: register for negative VSD4 fine tune adjustment.
V10RN[3:0]: register for negative VSD8 fine tune adjustment.
V11RN[3:0]: register for negative VSD20 fine tune adjustment.
V12RN[3:0]: register for negative VSD27 fine tune adjustment.
V13RN[3:0]: register for negative VSD36 fine tune adjustment.
V14RN[3:0]: register for negative VSD43 fine tune adjustment.
V15RN[3:0]: register for negative VSD55 fine tune adjustment.
V16RN[3:0]: register for negative VSD59 fine tune adjustment.

6.2.42. Base Image Number of Line (R400h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM. **Table 6-39** summarized the starting position for each SCN5-0 setting.

Table 6-39 (whenSM=0)

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G432
0	0	0	0	0	1	G9	G424
0	0	0	0	1	0	G17	G416
0	0	0	0	1	1	G25	G408
0	0	0	1	0	0	G33	G400
0	0	0	1	0	1	G41	G392
0	0	0	1	1	0	G49	G384
0	0	0	1	1	1	G57	G376
0	0	1	0	0	0	G65	G368
0	0	1	0	0	1	G73	G360
0	0	1	0	1	0	G81	G352
0	0	1	0	1	1	G89	G344
0	0	1	1	0	0	G97	G336
0	0	1	1	0	1	G105	G328
0	0	1	1	1	0	G113	G320
0	0	1	1	1	1	G121	G312
0	1	0	0	0	0	G129	G304
0	1	0	0	0	1	G137	G296
0	1	0	0	1	0	G145	G288
0	1	0	0	1	1	G153	G280
0	1	0	1	0	0	G161	G272
0	1	0	1	0	1	G169	G264
0	1	0	1	1	0	G177	G256
0	1	0	1	1	1	G185	G248
0	1	1	0	0	0	G193	G240
0	1	1	0	0	1	G201	G232
0	1	1	0	1	0	G209	G224
0	1	1	0	1	1	G217	G216
0	1	1	1	0	0	G225	G208
0	1	1	1	0	1	G233	G200
0	1	1	1	1	0	G241	G192
0	1	1	1	1	1	G249	G184
1	0	0	0	0	0	G257	G176
1	0	0	0	0	1	G265	G168
1	0	0	0	1	0	G273	G160
1	0	0	0	1	1	G281	G152
1	0	0	1	0	0	G289	G144
1	0	0	1	0	1	G297	G136
1	0	0	1	1	0	G305	G128
1	0	0	1	1	1	G313	G120
1	0	1	0	0	0	G321	G112
1	0	1	0	0	1	G329	G104
1	0	1	0	1	0	G337	G96
1	0	1	0	1	1	G345	G88
1	0	1	1	0	0	G353	G80
1	0	1	1	0	1	G361	G72
1	0	1	1	1	0	G369	G64
1	0	1	1	1	1	G377	G56
1	1	0	0	0	0	G385	G48
1	1	0	0	0	1	G393	G40
1	1	0	0	1	0	G401	G32
1	1	0	0	1	1	G409	G24
1	1	0	1	0	0	G417	G16
1	1	0	1	0	1	G425	G8
1	1	0	1	1	0	Setting disabled	
Setting disabled							
1	1	1	1	1	1	Setting disabled	

Table 6-40 (whenSM=1)

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G432
0	0	0	0	0	1	G17	G416
0	0	0	0	1	0	G33	G400
0	0	0	0	1	1	G49	G384
0	0	0	1	0	0	G65	G368
0	0	0	1	0	1	G81	G352
0	0	0	1	1	0	G97	G336
0	0	0	1	1	1	G113	G320
0	0	1	0	0	0	G129	G304
0	0	1	0	0	1	G145	G288
0	0	1	0	1	0	G161	G272
0	0	1	0	1	1	G177	G256
0	0	1	1	0	0	G193	G240
0	0	1	1	0	1	G209	G224
0	0	1	1	1	0	G225	G208
0	0	1	1	1	1	G241	G192
0	1	0	0	0	0	G257	G176
0	1	0	0	0	1	G273	G160
0	1	0	0	1	0	G289	G144
0	1	0	0	1	1	G305	G128
0	1	0	1	0	0	G321	G112
0	1	0	1	0	1	G337	G96
0	1	0	1	1	0	G353	G80
0	1	0	1	1	1	G369	G64
0	1	1	0	0	0	G385	G48
0	1	1	0	0	1	G401	G32
0	1	1	0	1	0	G417	G16
0	1	1	0	1	1	G2	G431
0	1	1	1	0	0	G18	G415
0	1	1	1	0	1	G34	G399
0	1	1	1	1	0	G50	G383
0	1	1	1	1	1	G66	G367
1	0	0	0	0	0	G82	G351
1	0	0	0	0	1	G98	G335
1	0	0	0	1	0	G114	G319
1	0	0	0	1	1	G130	G303
1	0	0	1	0	0	G146	G287
1	0	0	1	0	1	G162	G271
1	0	0	1	1	0	G178	G255
1	0	0	1	1	1	G194	G239
1	0	1	0	0	0	G210	G223
1	0	1	0	0	1	G226	G207
1	0	1	0	1	0	G242	G191
1	0	1	0	1	1	G258	G175
1	0	1	1	0	0	G274	G159
1	0	1	1	0	1	G290	G143
1	0	1	1	1	0	G306	G127
1	0	1	1	1	1	G322	G111
1	1	0	0	0	0	G338	G95
1	1	0	0	0	1	G354	G79
1	1	0	0	1	0	G370	G63
1	1	0	0	1	1	G386	G47
1	1	0	1	0	0	G402	G31
1	1	0	1	0	1	G418	G15
1	1	0	1	1	0	Setting disabled	
Setting disabled							
1	1	1	1	1	1		

NL5-0: Set the number of gate lines for different resolution of display panel. The combination of NL5-NL0 represents the gate line number are summarized at **Table 6-41**.

Table 6-41

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	No. of Lines	Driven gate lines
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	0	1	720 x 16 dots	16	G1 ~ G16
0	0	0	0	1	0	720 x 24 dots	24	G1 ~ G24
0	0	0	0	1	1	720 x 32 dots	32	G1 ~ G32
0	0	0	1	0	0	720 x 40 dots	40	G1 ~ G40
0	0	0	1	0	1	720 x 48 dots	48	G1 ~G48
0	0	0	1	1	0	720 x 56 dots	56	G1 ~ G56
0	0	0	1	1	1	720 x 64 dots	64	G1 ~ G64
0	0	1	0	0	0	720 x 72 dots	72	G1 ~ G72
0	0	1	0	0	1	720 x 80 dots	80	G1 ~ G80
0	0	1	0	1	0	720 x 88 dots	88	G1 ~ G88
0	0	1	0	1	1	720 x 96 dots	96	G1 ~ G96
0	0	1	1	0	0	720 x 104 dots	104	G1 ~ G104
0	0	1	1	0	1	720 x 112 dots	112	G1 ~ 112
0	0	1	1	1	0	720 x 120 dots	120	G1 ~ 120
0	0	1	1	1	1	720 x 128 dots	128	G1 ~ 128
0	1	0	0	0	0	720 x 136 dots	136	G1 ~ 136
0	1	0	0	0	1	720 x 144 dots	144	G1 ~ 144
0	1	0	0	1	0	720 x 152 dots	152	G1 ~ 152
0	1	0	0	1	1	720 x 160 dots	160	G1 ~ 160
0	1	0	1	0	0	720 x 168 dots	168	G1 ~ 168
0	1	0	1	0	1	720 x 176 dots	176	G1 ~ 176
0	1	0	1	1	0	720 x 184 dots	184	G1 ~ 184
0	1	0	1	1	1	720 x 192 dots	192	G1 ~ 192
0	1	1	0	0	0	720 x 200 dots	200	G1 ~ 200
0	1	1	0	0	1	720 x 208 dots	208	G1 ~ 208
0	1	1	0	1	0	720 x 216 dots	216	G1 ~ 216
0	1	1	0	1	1	720 x 224 dots	224	G1 ~ 224
0	1	1	1	0	0	720 x 232 dots	232	G1 ~ 232
0	1	1	1	0	1	720 x 240 dots	240	G1 ~ 240
0	1	1	1	1	0	720 x 248 dots	248	G1 ~ 248
0	1	1	1	1	1	720 x 256 dots	256	G1 ~ 256
1	0	0	0	0	0	720 x 264 dots	264	G1 ~ 264
1	0	0	0	0	1	720 x 272 dots	272	G1 ~ 272
1	0	0	0	1	0	720 x 280 dots	280	G1 ~ 280
1	0	0	0	1	1	720 x 288 dots	288	G1 ~ 288
1	0	0	1	0	0	720 x 296 dots	296	G1 ~ 296
1	0	0	1	0	1	720 x 304 dots	304	G1 ~ 304
1	0	0	1	1	0	720 x 312 dots	312	G1 ~ 312
1	0	0	1	1	1	720 x 320 dots	320	G1 ~ 320
1	0	1	0	0	0	720 x 328 dots	328	G1 ~ 328

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	No. of Lines	Driven gate lines
1	0	1	0	0	1	720 x 336 dots	336	G1 ~ 336
1	0	1	0	1	0	720 x 344 dots	344	G1 ~ 344
1	0	1	0	1	1	720 x 352 dots	352	G1 ~ 352
1	0	1	1	0	0	720 x 360 dots	360	G1 ~ 360
1	0	1	1	0	1	720 x 368 dots	368	G1 ~ 368
1	0	1	1	1	0	720 x 376 dots	376	G1 ~ 376
1	0	1	1	1	1	720 x 384 dots	384	G1 ~ 384
1	1	0	0	0	0	720 x 392 dots	392	G1 ~ 392
1	1	0	0	0	1	720 x 400 dots	400	G1 ~ 400
1	1	0	0	1	0	720 x 408 dots	408	G1 ~ 408
1	1	0	0	1	1	720 x 416 dots	416	G1 ~ 416
1	1	0	1	0	0	720 x 424 dots	424	G1 ~ 424
1	1	0	1	0	1	720 x 432 dots	432	G1 ~ 432
Setting Disabled								

Note: Back porch and a front porch (set with BP/FP bits respectively) are inserted before/ after driving all gate lines.

GS: Shift direction of the gate driver output selection. When
GS="0", gate driver shift from G1 to G432. When GS = "1", gate driver shift from G432 to G1.

6.2.43. Base Image Display Control (R401h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input. **Table 6-42** summarized REV bit function.

Table 6-42

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000 ⋮ 18'h3FFFF	V63 ⋮ V0	V0 ⋮ V63
1	18'h00000 ⋮ 18'h3FFFF	V0 ⋮ V63	V63 ⋮ V0

VLE: OTM4001A provides vertical scrolling function which can be set by VLE bit.
VLE = "1", vertical scrolling function enable. The amout of scrolling line from the first line is determined by VL[8:0].
VLE = "0", normal display.

NDL: set the source driver output level in non-lit area..
NDL = "1", Positive = V0, Negative = V31;
NDL = "0", Postive = V31 and Negative = V0.

6.2.44. Based Image Vertical Scroll Control (R404h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)

VL8-0: OTM4001A provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 6-43** summarized the function of VL8-0 setting.

Table 6-43

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	1	0	1	0	1	1	1	0	431 lines
1	1	0	1	0	1	1	1	1	432 lines

Note: VL8-0 bits cannot set more than 432 lines.

6.2.45. Display Position - Partial Display 1 (R500h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00

See R505h.

6.2.46. RAM Address Start – Partial Display 1 (R501h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A08	PTS A07	PTS A06	PTS A05	PTS A04	PTS A03	PTS A02	PTS A01	PTS A00

See R505h.

6.2.47. RAM Address End – Partail Display 1 (R502h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A08	PTE A07	PTE A06	PTE A05	PTE A04	PTE A03	PTE A02	PTE A01	PTE A00

See R505h.

6.2.48. Display Position – Partial Display 2 (R503h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10

See R505h.

6.2.49. RAM Address Start – Partial Display 2 (R504h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10

See R505h.

6.2.50. RAM Address End – Partial Display 2 (R505h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Make sure PTSA0≤PTEA0.

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Make sure PTSA1≤PTEA1.

6.2.51. CABC Gamma RAM Bank Selection (R601h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	CABC_BANK2	CABC_BANK1	CABC_BANK0

CABC_BANK[2:0] : Select which bank is selected to read data out.

6.2.52. CABC Gamma RAM Bank Write (R602h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	CABC RAM Write Command															

Start to write the cabc gamma data to cabc gamma ram.

6.2.53. CABC Gamma RAM Bank Read (R603h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	CABC RAM Read Command															

Start to Read the cabc gamma data to cabc gamma ram.

6.2.54. Pin Control (R606h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	TCREV 1(0)	0	0	0	0	0	0	0	TCREV 0(0)

TCREV1-0: Set the order of receiving data when using i80 interface.

TCREV1-0	2 Transfers/Pixel	3 Transfers/Pixel
00	1st to 2nd	1st to 3rd
01 – 10	Setting Disabled	
11	2nd to 1st	3rd to 1st

Note 1: During read operation, the setting of TCREV is ignored; data is transferred from 1st to 2nd/1st to 3rd.

Note 2: Reset TCREV after reset and power-on.

7. GRAM

Table 7-1 GRAM address and display panel position (SS = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G400	"00000"H			"00001"H			"00002"H			"00003"H			....	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G399	"00100"H			"00101"H			"00102"H			"00103"H			....	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G398	"00200"H			"00201"H			"00202"H			"00203"H			....	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G397	"00300"H			"00301"H			"00302"H			"00303"H			....	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G396	"00400"H			"00401"H			"00402"H			"00403"H			....	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G395	"00500"H			"00501"H			"00502"H			"00503"H			....	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G394	"00600"H			"00601"H			"00602"H			"00603"H			....	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G393	"00700"H			"00701"H			"00702"H			"00703"H			....	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G392	"00800"H			"00801"H			"00802"H			"00803"H			....	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G391	"00900"H			"00901"H			"00902"H			"00903"H			....	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G390	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G12	G389	"00B00"H			"00B01"H			"00B02"H			"00B03"H			....	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G388	"00C00"H			"00C01"H			"00C02"H			"00C03"H			....	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G387	"00D00"H			"00D01"H			"00D02"H			"00D03"H			....	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G386	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G385	"00F00"H			"00F01"H			"00F02"H			"00F03"H			....	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G384	"01000"H			"01001"H			"01002"H			"01003"H			....	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G383	"01100"H			"01101"H			"01102"H			"01103"H			....	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G382	"01200"H			"01201"H			"01202"H			"01203"H			....	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G381	"01300"H			"01301"H			"01302"H			"01303"H			....	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G393	G8	"1A900"H			"1A801"H			"1A802"H			"1A803"H			....	"1A8EC"H			"1A8ED"H			"1A8EE"H			"1A8EF"H		
G394	G7	"1AA00"H			"1A901"H			"1A902"H			"1A903"H			....	"1A9EC"H			"1A9ED"H			"1A9EE"H			"1A9EF"H		
G395	G6	"1AB00"H			"1AA01"H			"1AA02"H			"1AA03"H			....	"1AAEC"H			"1AAED"H			"1AAEE"H			"1AAEF"H		
G396	G5	"1AC00"H			"1AB01"H			"1AB02"H			"1AB03"H			....	"1ABEC"H			"1ABED"H			"1ABEE"H			"1ABEF"H		
G397	G4	"1AD00"H			"1AC01"H			"1AC02"H			"1AC03"H			....	"1ACEC"H			"1ACED"H			"1ACEE"H			"1ACEF"H		
G398	G3	"1AD00"H			"1AD01"H			"1AD02"H			"1AD03"H			....	"1ADEC"H			"1ADED"H			"1ADEE"H			"1ADEF"H		
G399	G2	"1AE00"H			"1AE01"H			"1AE02"H			"1AE03"H			....	"1AEEC"H			"1AEED"H			"1AEEE"H			"1AEEF"H		
G400	G1	"1AF00"H			"1AF01"H			"1AF02"H			"1AF03"H			....	"1AFEC"H			"1AFED"H			"1AFEE"H			"1AFEF"H		

Table 7-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G432	"000EF"H			"000EE"H			"000ED"H			"000EC"H			….	"00003"H			"00002"H			"00001"H			"00000"H		
G2	G431	"001EF"H			"001EE"H			"001ED"H			"001EC"H			….	"00103"H			"00102"H			"00101"H			"00100"H		
G3	G430	"002EF"H			"002AE"H			"002ED"H			"002EC"H			….	"00203"H			"00202"H			"00201"H			"00200"H		
G4	G429	"003EF"H			"003EE"H			"003ED"H			"003EC"H			….	"00303"H			"00302"H			"00301"H			"00300"H		
G5	G428	"004EF"H			"004EE"H			"004ED"H			"004EC"H			….	"00403"H			"00402"H			"00401"H			"00400"H		
G6	G427	"005EF"H			"005EE"H			"005ED"H			"005EC"H			….	"00503"H			"00502"H			"00501"H			"00500"H		
G7	G426	"006EF"H			"006EE"H			"006ED"H			"006EC"H			….	"00603"H			"00602"H			"00601"H			"00600"H		
G8	G425	"007EF"H			"007EE"H			"007ED"H			"007EC"H			….	"00703"H			"00702"H			"00701"H			"00700"H		
G9	G424	"008EF"H			"008EE"H			"008ED"H			"008EC"H			….	"00803"H			"00802"H			"00801"H			"00800"H		
G10	G423	"009EF"H			"009EE"H			"009ED"H			"009EC"H			….	"00903"H			"00902"H			"00901"H			"00900"H		
G11	G422	"00AEF"H			"00AEE"H			"00AED"H			"00AEC"H			….	"00E03"H			"00A02"H			"00A01"H			"00A00"H		
G12	G421	"00BEF"H			"00BEE"H			"00BED"H			"00BEC"H			….	"00B03"H			"00B02"H			"00B01"H			"00B00"H		
G13	G420	"00CEF"H			"00CEE"H			"00CED"H			"00CEC"H			….	"00C03"H			"00C02"H			"00C01"H			"00C00"H		
G14	G419	"00DEF"H			"00DEE"H			"00DED"H			"00DEC"H			….	"00D03"H			"00D02"H			"00D01"H			"00D00"H		
G15	G418	"00EEF"H			"00EEE"H			"00EED"H			"00EEC"H			….	"00E03"H			"00E02"H			"00E01"H			"00E00"H		
G16	G417	"00FEF"H			"00FEE"H			"00FED"H			"00FEC"H			….	"00F03"H			"00F02"H			"00F01"H			"00F00"H		
G17	G416	"010EF"H			"010EE"H			"010ED"H			"010EC"H			….	"01003"H			"01002"H			"01001"H			"01000"H		
G18	G415	"011EF"H			"011EE"H			"011ED"H			"011EC"H			….	"01103"H			"01102"H			"01101"H			"01100"H		
G19	G414	"012EF"H			"012EE"H			"012ED"H			"012EC"H			….	"01203"H			"01202"H			"01201"H			"01200"H		
G20	G413	"013EF"H			"013EE"H			"013ED"H			"013EC"H			….	"01303"H			"01302"H			"01301"H			"01300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G425	G8	"1A8EF"H			"1A8EE"H			"1A8ED"H			"1A8EC"H			….	"1A803"H			"1A802"H			"1A801"H			"1A900"H		
G426	G7	"1A9EF"H			"1A9EE"H			"1A9ED"H			"1A9EC"H			….	"1A903"H			"1A902"H			"1A901"H			"1AA00"H		
G427	G6	"1AAEF"H			"1AAEE"H			"1AAED"H			"1AAEC"H			….	"1AA03"H			"1AA02"H			"1AA01"H			"1AB00"H		
G428	G5	"1ABEF"H			"1ABEE"H			"1ABED"H			"1ABEC"H			….	"1AB03"H			"1AB02"H			"1AB01"H			"1AC00"H		
G429	G4	"1ACEF"H			"1ACEE"H			"1ACED"H			"1ACEC"H			….	"1AC03"H			"1AC02"H			"1AC01"H			"1AD00"H		
G430	G3	"1ADEF"H			"1ADEE"H			"1ADED"H			"1ADEC"H			….	"1AD03"H			"1AD02"H			"1AD01"H			"1AD00"H		
G431	G2	"1AEEF"H			"1AEEE"H			"1AEED"H			"1AEEC"H			….	"1AE03"H			"1AE02"H			"1AE01"H			"1AE00"H		
G432	G1	"1AFEF"H			"1AFEE"H			"1AFED"H			"1AFEC"H			….	"1AF03"H			"1AF02"H			"1AF01"H			"1AF00"H		

8. INTERFACES

The OTM4001A provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, OTM4001A provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 8-1** summarized different interfaces for different display requirement.

Table 8-1

Operation Mode	Display Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
System	Still picture	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1)	Moving picture	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2)	Rewriting still pictures while displaying moving pictures	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface	Moving pictures	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

8.1. System Interface

The system interfaces of OTM4001A can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM2/1/0 pins. The system interface can set instructions and access RAM. **Table 8-2** summarized the interface corresponding to IM2-0 setting.

Table 8-2

IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	80-system 18-bit interface	DB17 to 0
0	0	1	80-system 9-bit interface	DB17 to 9
0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	1	1	80-system 8-bit interface	DB17 to 10
1	0	*	Serial peripheral interface (SPI)	DB1 to 0
1	1	0	Setting disabled	-
1	1	1	Setting disabled	-

8.1.1. 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 8-1** and **Figure 8-2**, respectively.

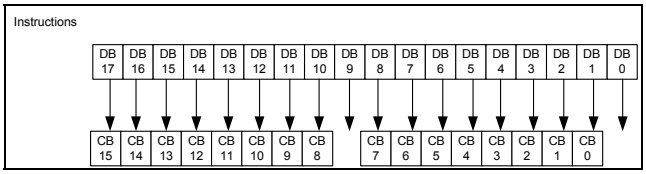


Figure 8-1

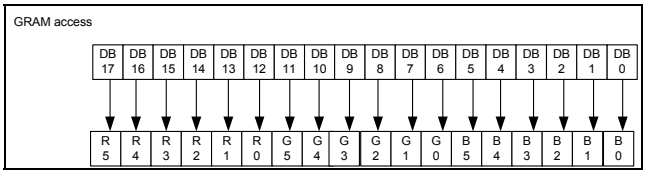


Figure 8-2

8.1.2. 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 8-3** and **Figure 8-4**, respectively.

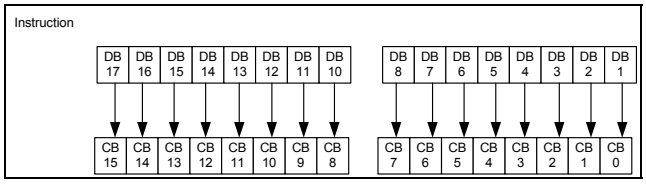


Figure 8-3

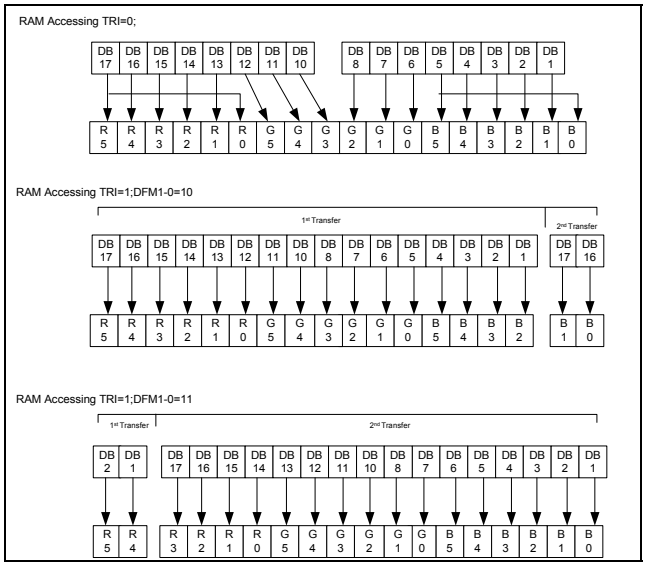


Figure 8-4

8.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 8-5** and **Figure 8-6**, respectively.

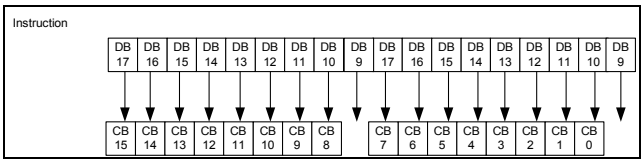


Figure 8-5

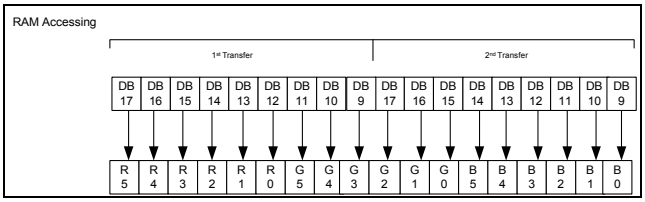


Figure 8-6

8.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 8-7** and **Figure 8-8**, respectively.

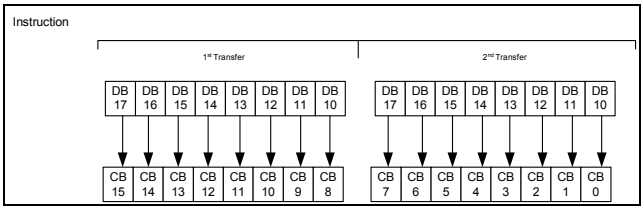


Figure 8-7

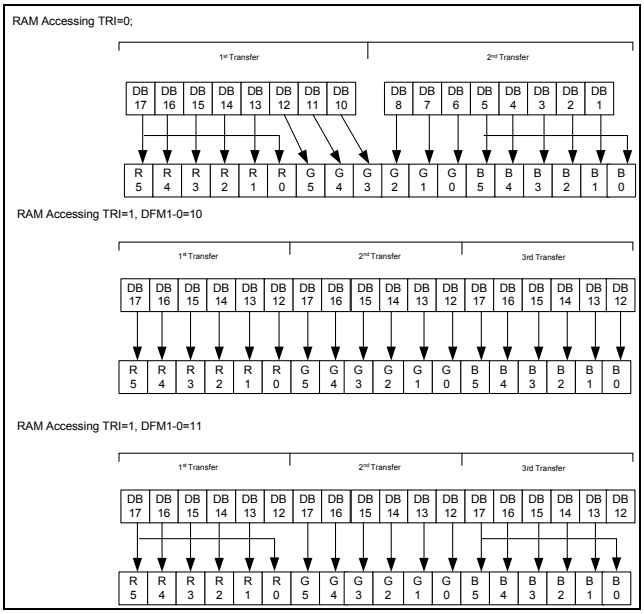


Figure 8-8

8.1.5. Serial Peripheral interface (SPI)

The system interface of OTM4001A also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and OTM4001A. IM0/ID pin served as the ID pin. **Figure 8-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 8-10** and **Figure 8-11**, respectively.

When read operation is desired In SPI mode, valid data are read out as the OTM4001A reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with TRI=1/ DFM1-0=10 and status read are illustrated in **Figure 8-12**, **Figure 8-13** and **Figure 8-14**, respectively.

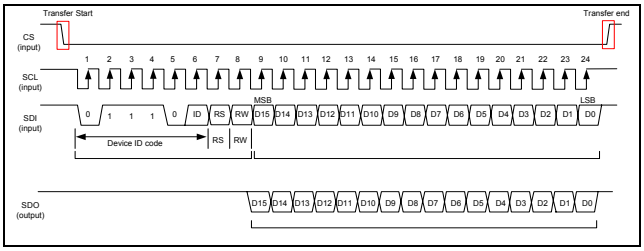


Figure 8-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

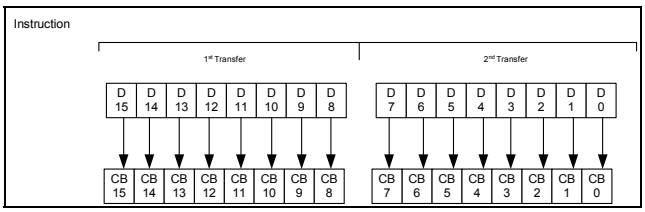


Figure 8-10

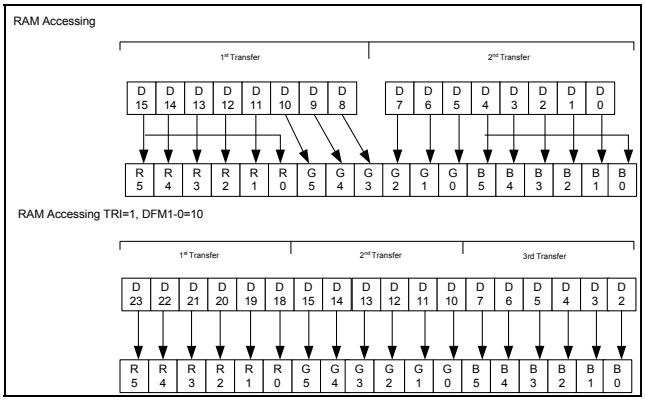


Figure 8-11

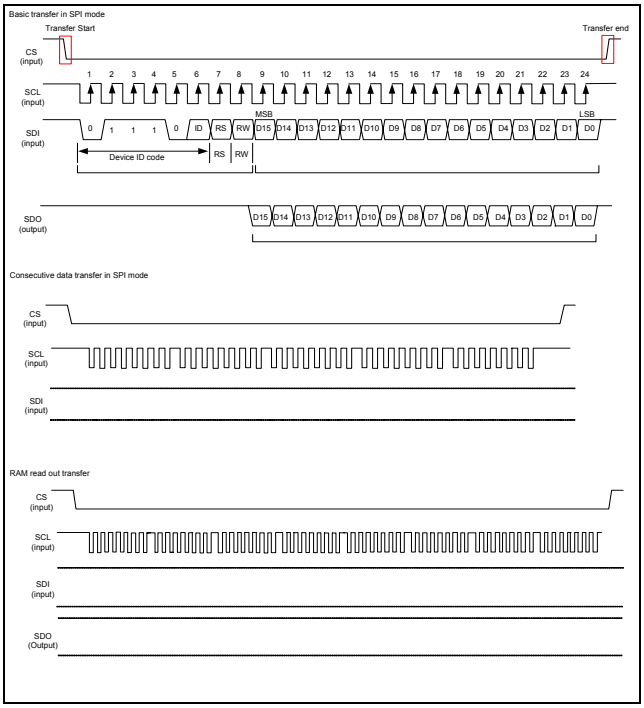


Figure 8-12

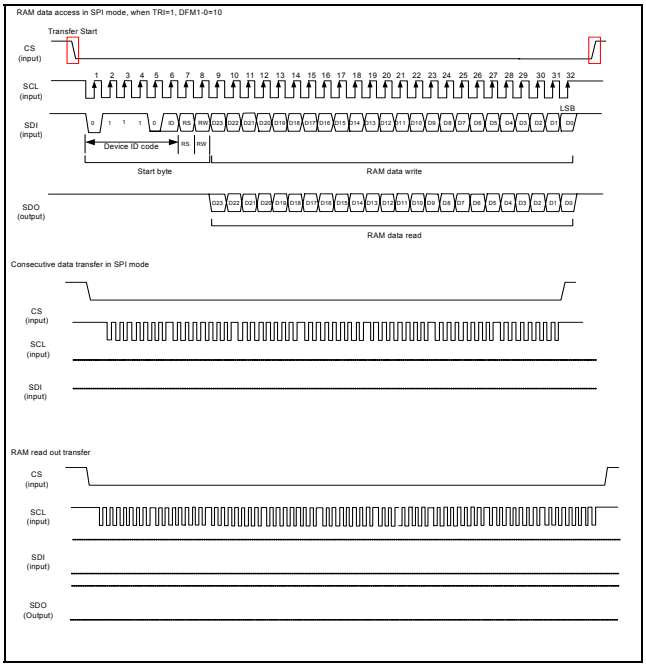


Figure 8-13

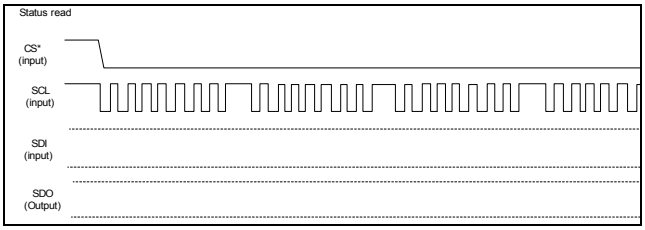


Figure 8-14

8.2. VSYNC Interface

The OTM4001A also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = “10” and RM = “0” can initialized VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 8-15** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. OTM4001A can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

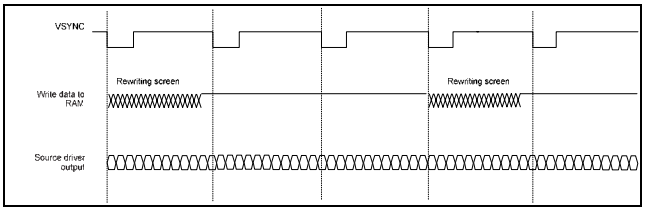


Figure 8-15

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

Input clock frequency = FrameRate x (DisplayLines + FrontPorch + BackPorch) x 16 x variance

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

8.3. External Display Interface

OTM4001A also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 8-3** summarized the corresponding types of RGB interface with RM1-0 setting.

Table 8-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

RGB interface cab access OTM4001A by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 8-16** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions,

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface.

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB-I/F mode, while writing data to the internal RAM make sure to use the high-speed write mode (HWM = “1”)

(e) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(f) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

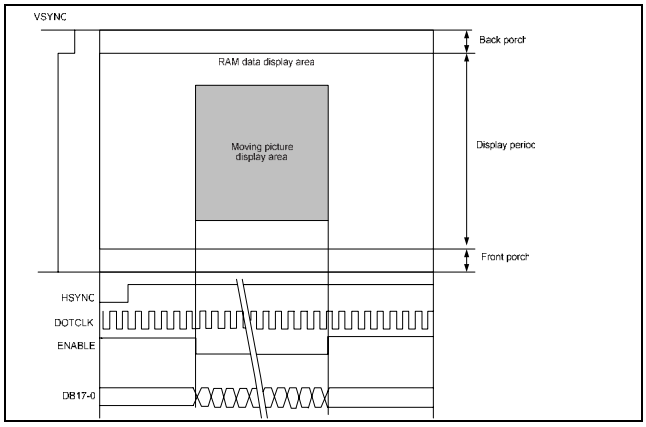


Figure 8-16

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 8-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 8-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

OTM4001A can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interfaces are shown in **Figure 8-17** and **Figure 8-18** respectively.

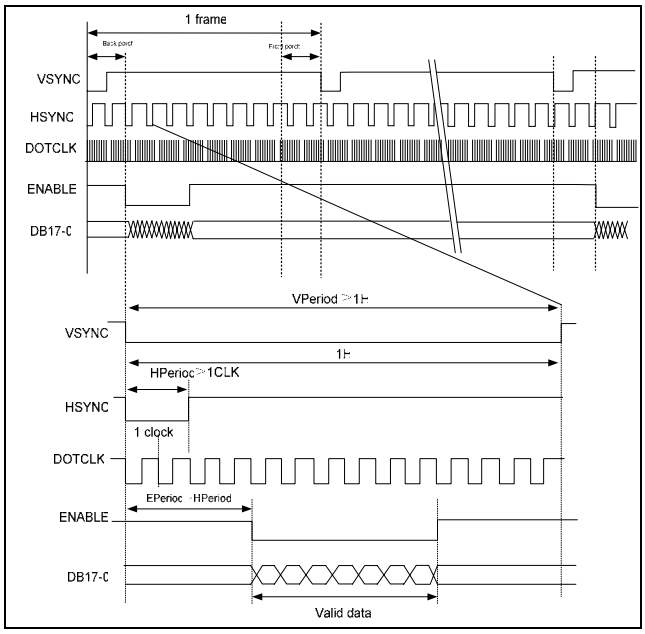


Figure 8-17

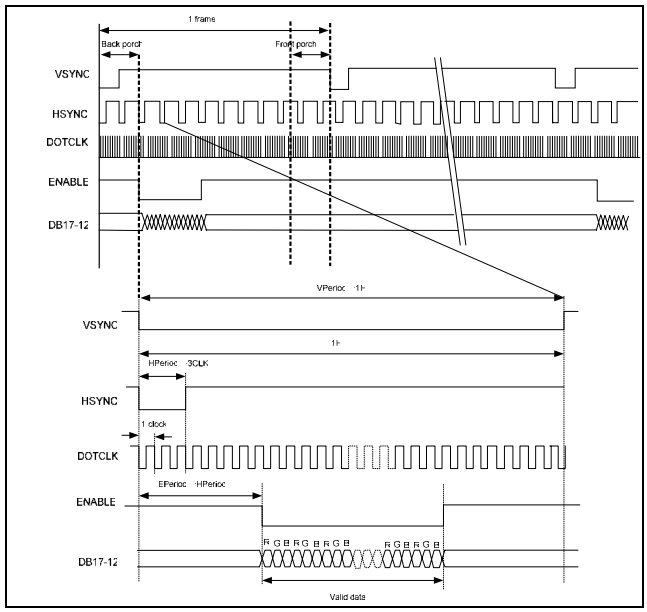


Figure 8-18

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access CBIe through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 8-19 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

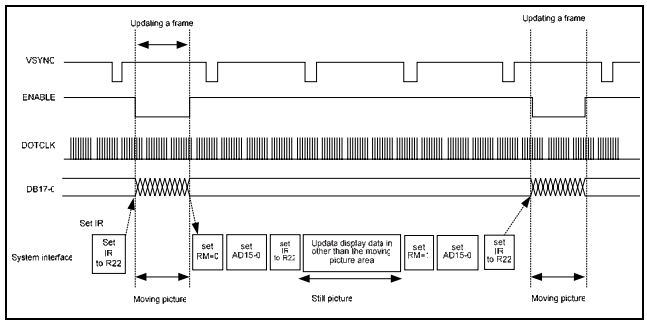


Figure 8-19

8.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 8-20** and **Figure 8-21**, respectively.

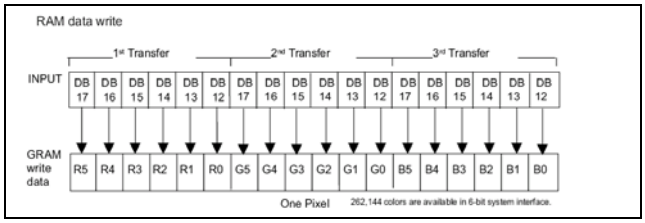


Figure 8-20

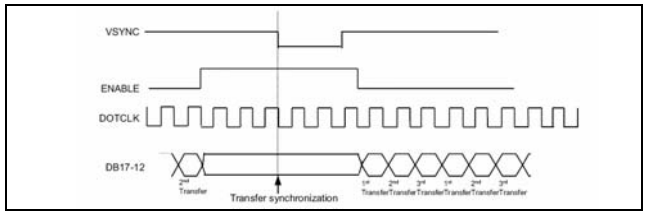


Figure 8-21

8.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 8-22**.

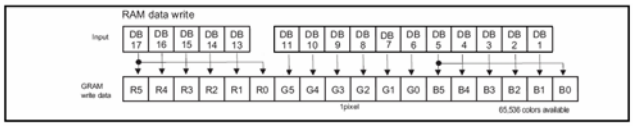


Figure 8-22

8.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 8-23**.

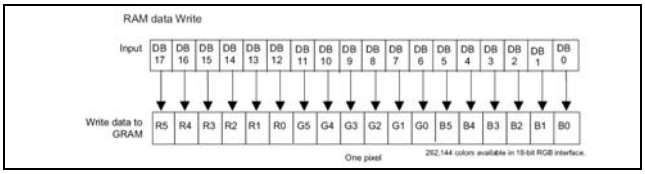


Figure 8-23

9. Display Feature Function:

9.1. FMARK function:

OTM4001A provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCD display can avoid flicker effect. FMARK output position and onterval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 9-1 illustrated the FMARK output position when FMP[8:0]=9'h008.

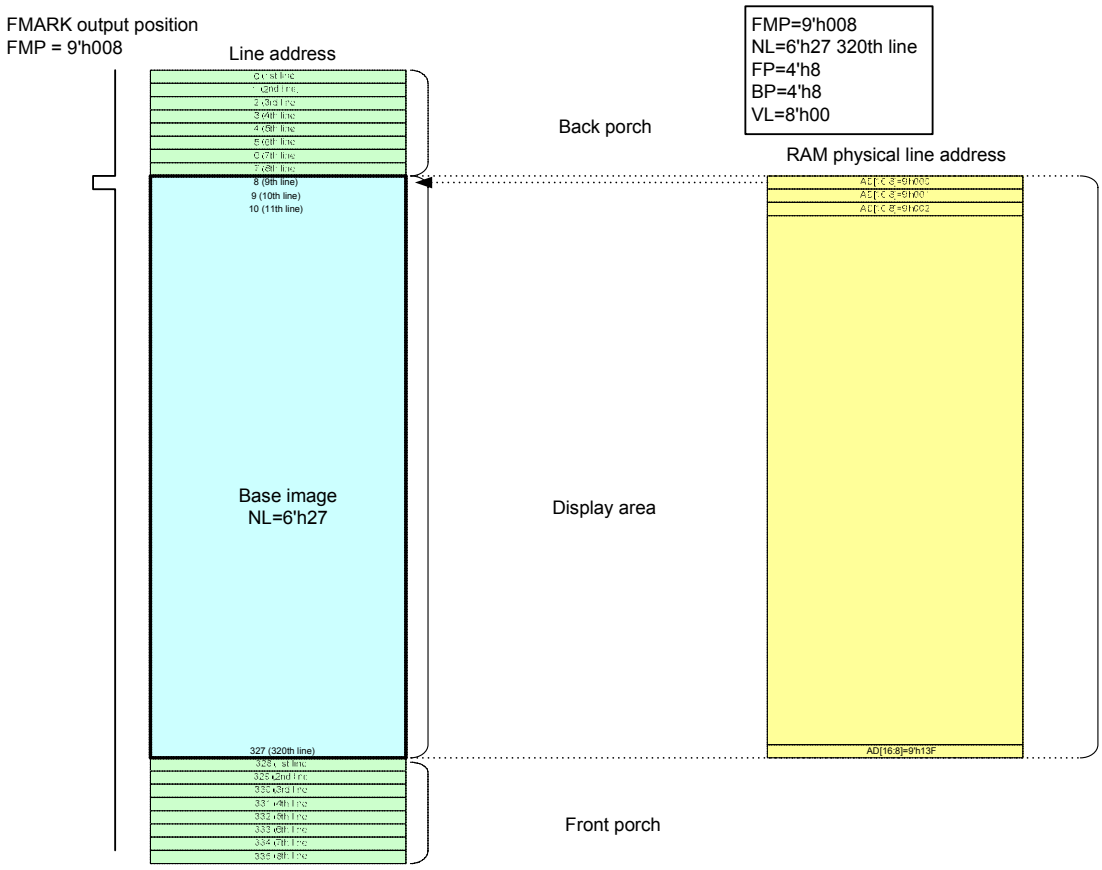
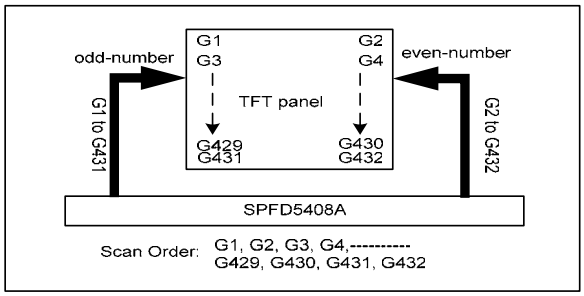
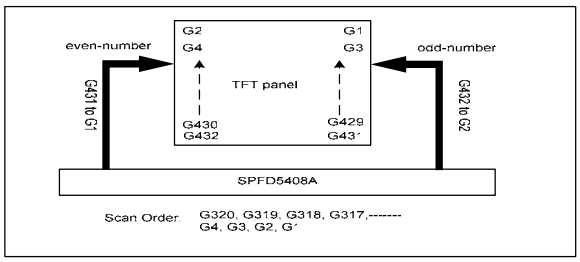
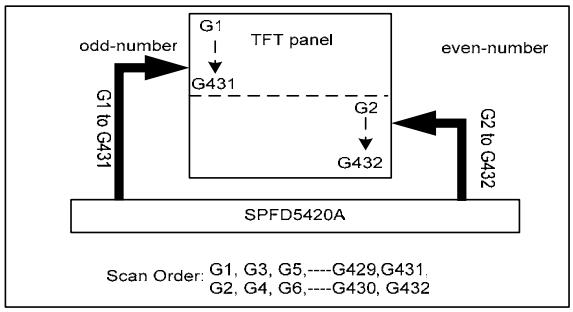
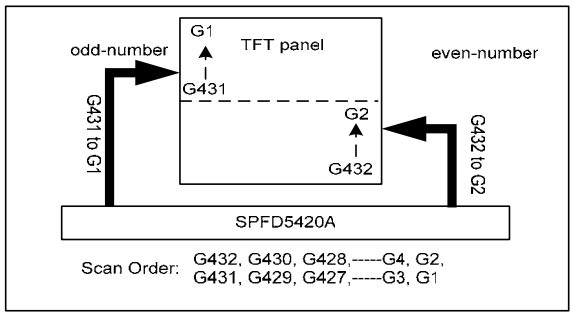


Figure 9-1 Example of FMARK signal.

9.2. Scan Mode function:

SM	GS	Scan Direction
0	0	
0	1	
1	0	
1	1	

9.3. Partial Display function:

OTM4001A has partial display function feature which can provide only partial display for power saving purpose. Partial display function can be accessed by setting BSEE="0",. Moreover, 2 partial display area (partial image 1/ partial image 2) can be initialized by setted PTDE0="1" and PTDE1="1", respectively. The partial display area for partial image 1 and partial 2 can be set by PTSA0 / PTEA0 and PTSA1/ PTEA1, respectively. **Table 9-1** and **Figure 9-2** summarized the full and partial display function.

Table 9-1 Partial display function summary table

Case	Function Setting	Display area setting	Display Position
Full dsiplay	**BASEE="1"** **PTDE0="x"** **PTDE1="x"**	**(BSA,BEA)**	**-**
Partail image1:0n **Partial image2:Off**	**BASEE="0"** **PTDE0="1"** **PTDE1="0"**	**(PTSA0,PTEA0)**	**PTDP0**
Partail image1:Off **Partial image2:On**	**BASEE="0"** **PTDE0="0"** **PTDE1="1"**	**(PTSA1,PTEA1)**	**PTDP1**
Partail image1:On **Partial image2:On**	**BASEE="0"** **PTDE0="1"** **PTDE1="1"**	**(PTSA0,PTEA0)** **(PTSA1,PTEA1)**	**PTDP0 & PTDP1**

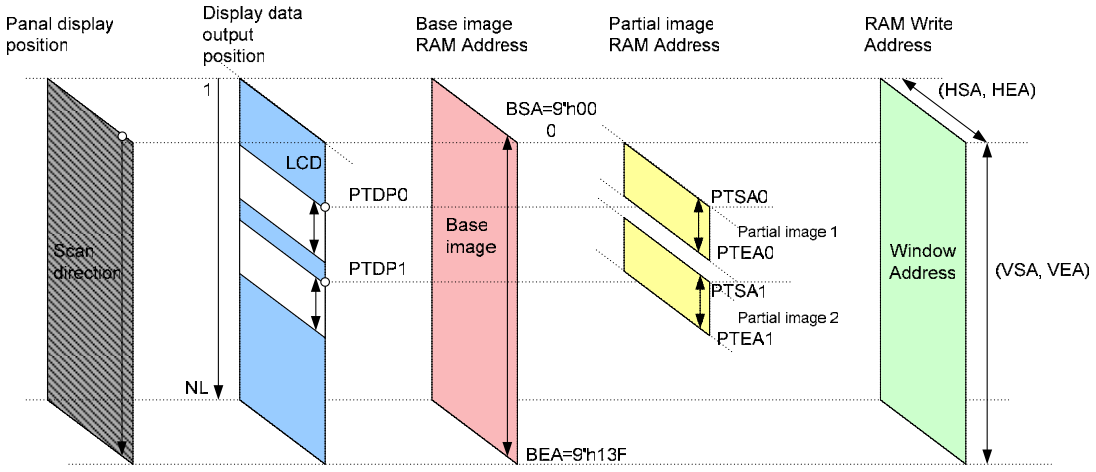


Figure 9-2 Partial display function diagram

Figure 9-3 indicated the case of NL[5:0] setting is < 6'h35 which active line is less than 432. Partial display image data can stored in not active area.

Figure 9-4 indicated the partial display area start position. The partial display area and start position can be set by (**PTSA0, PTEA0 , PTSA1, PTEA1) and (PTDP0, PTDP1).**

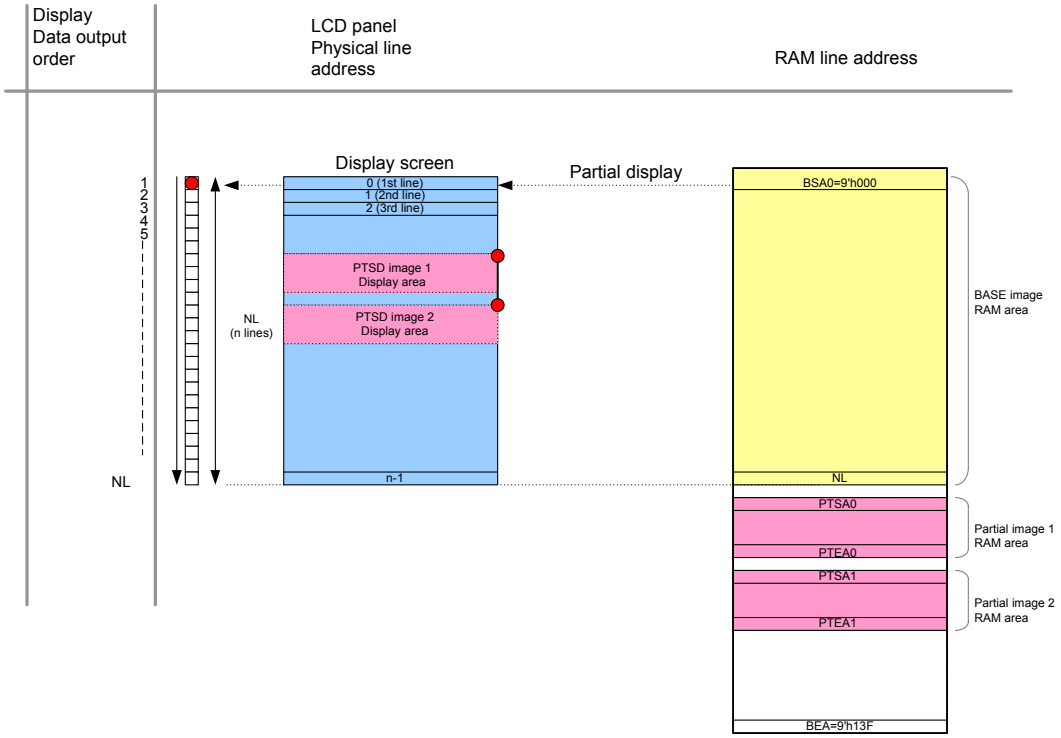


Figure 9-3 Example of NL[5:0] setting is < 6'h35 case

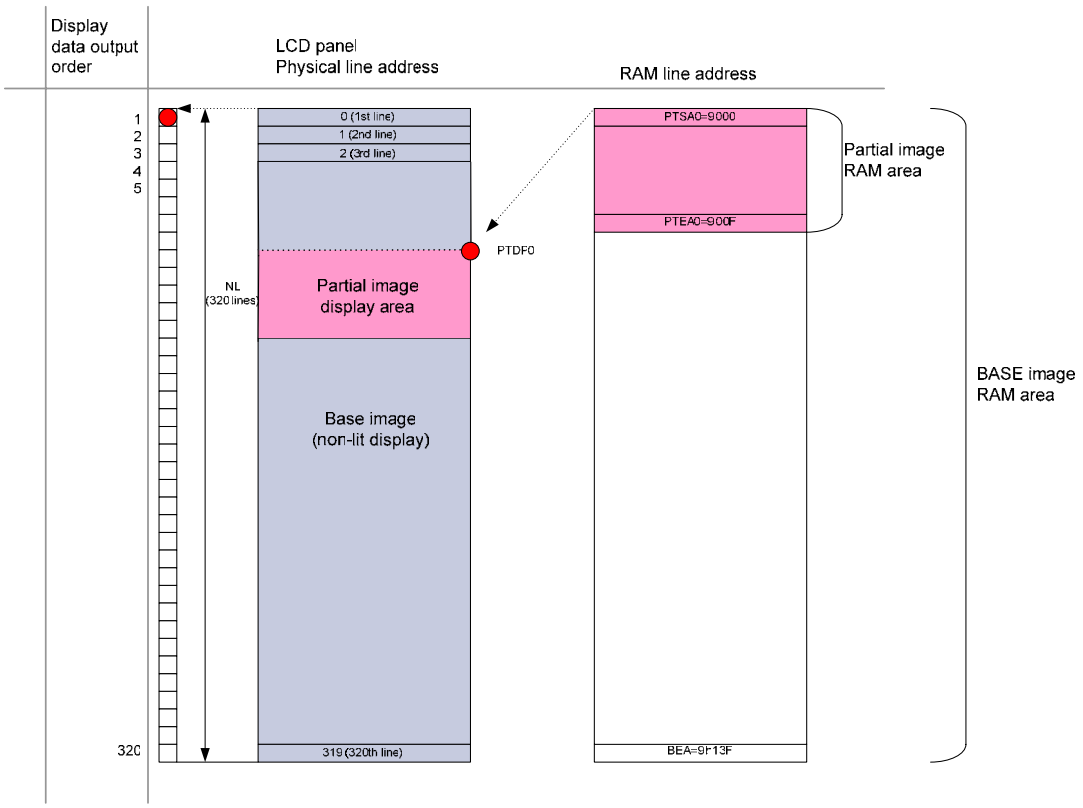


Figure 9-4 indicated the partial display area start position.

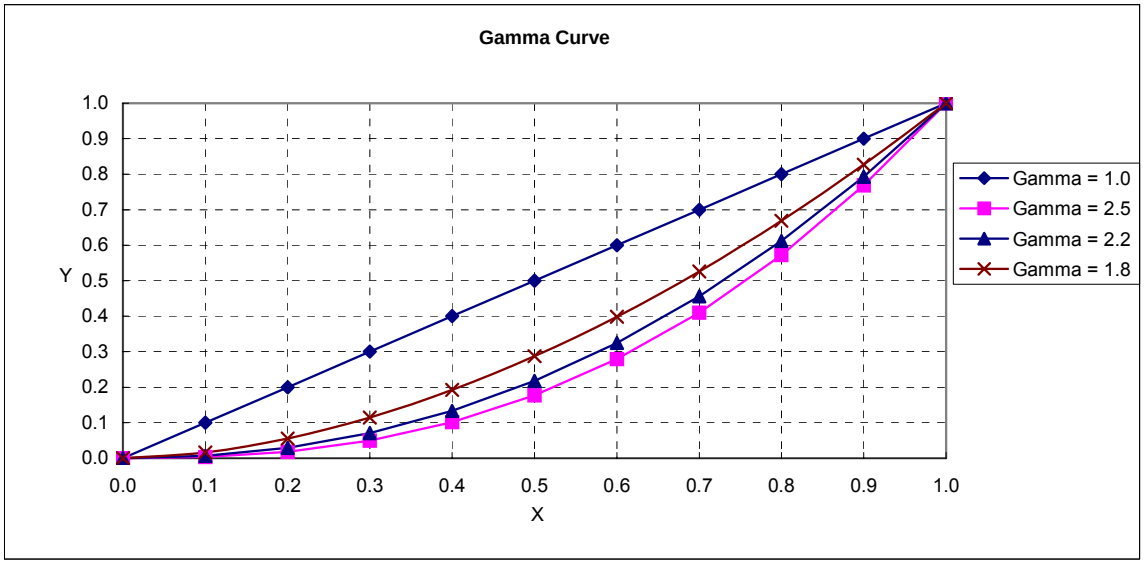
9.4. Gamma Correction functions:

OTM4001A adopt Gamma voltage generation circuit which can provide wider output voltage range to fit the different kind of liquid crystal for Gamma curve from 1.0~2.5. The Gamma output voltage can be set by R300h~R3F0h.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment
V7RP[4:0]: register for positive VSD13 fine tune adjustment
V8RP[4:0]: register for positive VSD50 fine tune adjustment
V9RP[3:0]: register for positive VSD4 fine tune adjustment
V10RP[3:0]: register for positive VSD8 fine tune adjustment
V11RP[3:0]: register for positive VSD20 fine tune adjustment
V12RP[3:0]: register for positive VSD27 fine tune adjustment
V13RP[3:0]: register for positive VSD36 fine tune adjustment
V14RP[3:0]: register for positive VSD43 fine tune adjustment
V15RP[3:0]: register for positive VSD55 fine tune adjustment
V16RP[3:0]: register for positive VSD59 fine tune adjustment

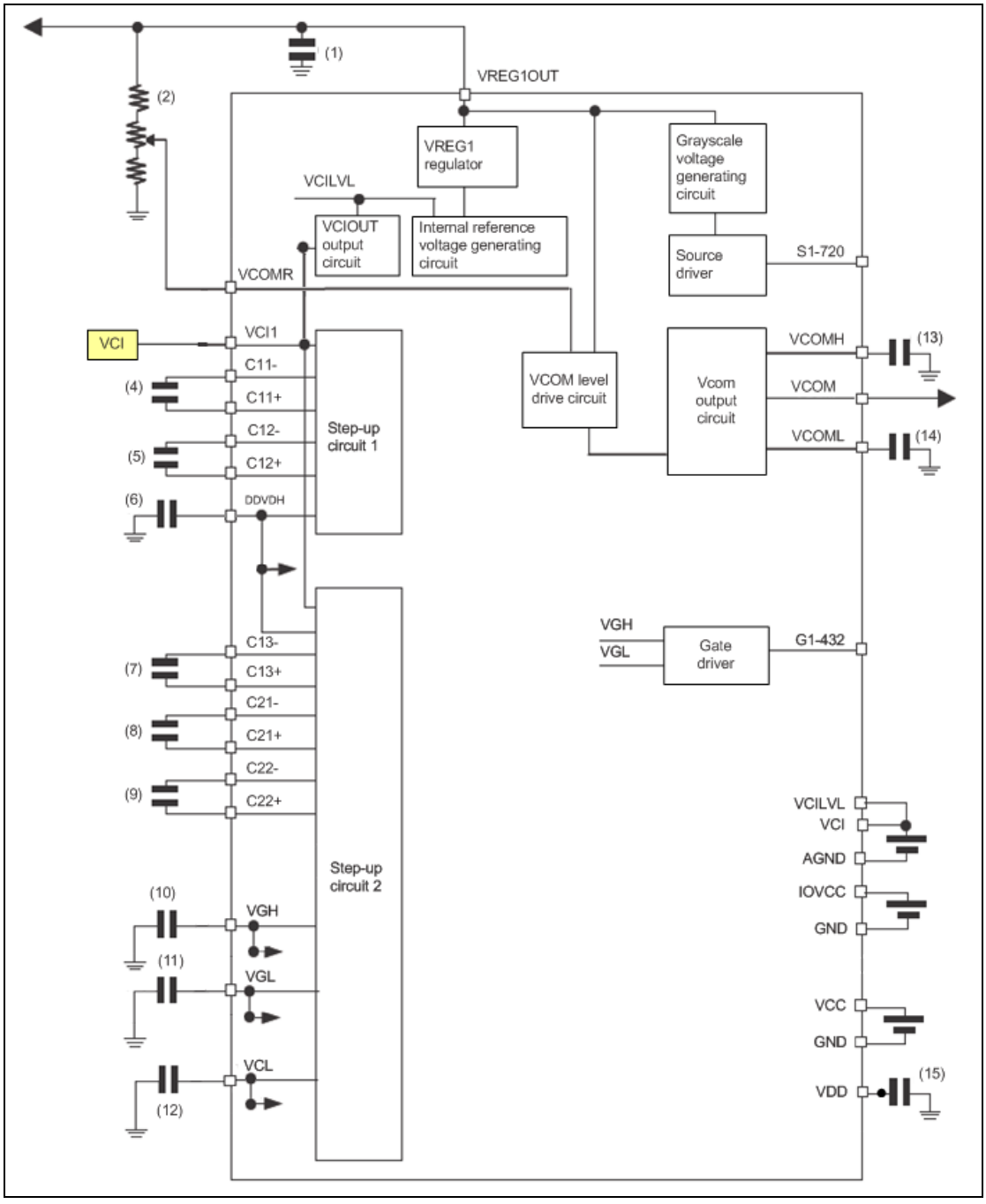
V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment
V7RN[4:0]: register for negative VSD13 fine tune adjustment
V8RN[4:0]: register for negative VSD50 fine tune adjustment
V9RN[3:0]: register for negative VSD4 fine tune adjustment
V10RN[3:0]: register for negative VSD8 fine tune adjustment
V11RN[3:0]: register for negative VSD20 fine tune adjustment
V12RN[3:0]: register for negative VSD27 fine tune adjustment
V13RN[3:0]: register for negative VSD36 fine tune adjustment
V14RN[3:0]: register for negative VSD43 fine tune adjustment
V15RN[3:0]: register for negative VSD55 fine tune adjustment
V16RN[3:0]: register for negative VSD59 fine tune adjustment

Figure 9-5 illustrated 4 different Gamma Curve.

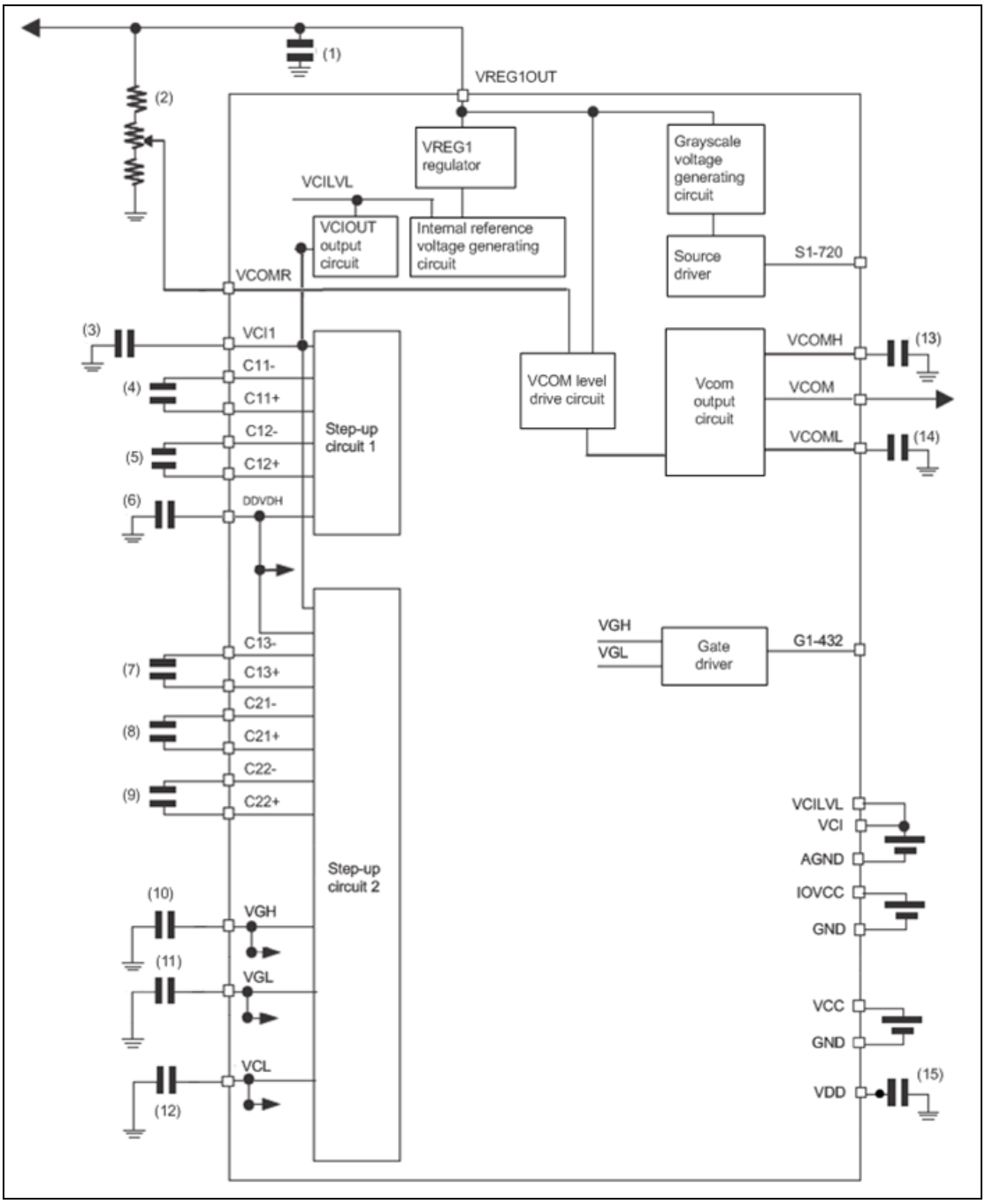


10. Power Management System:

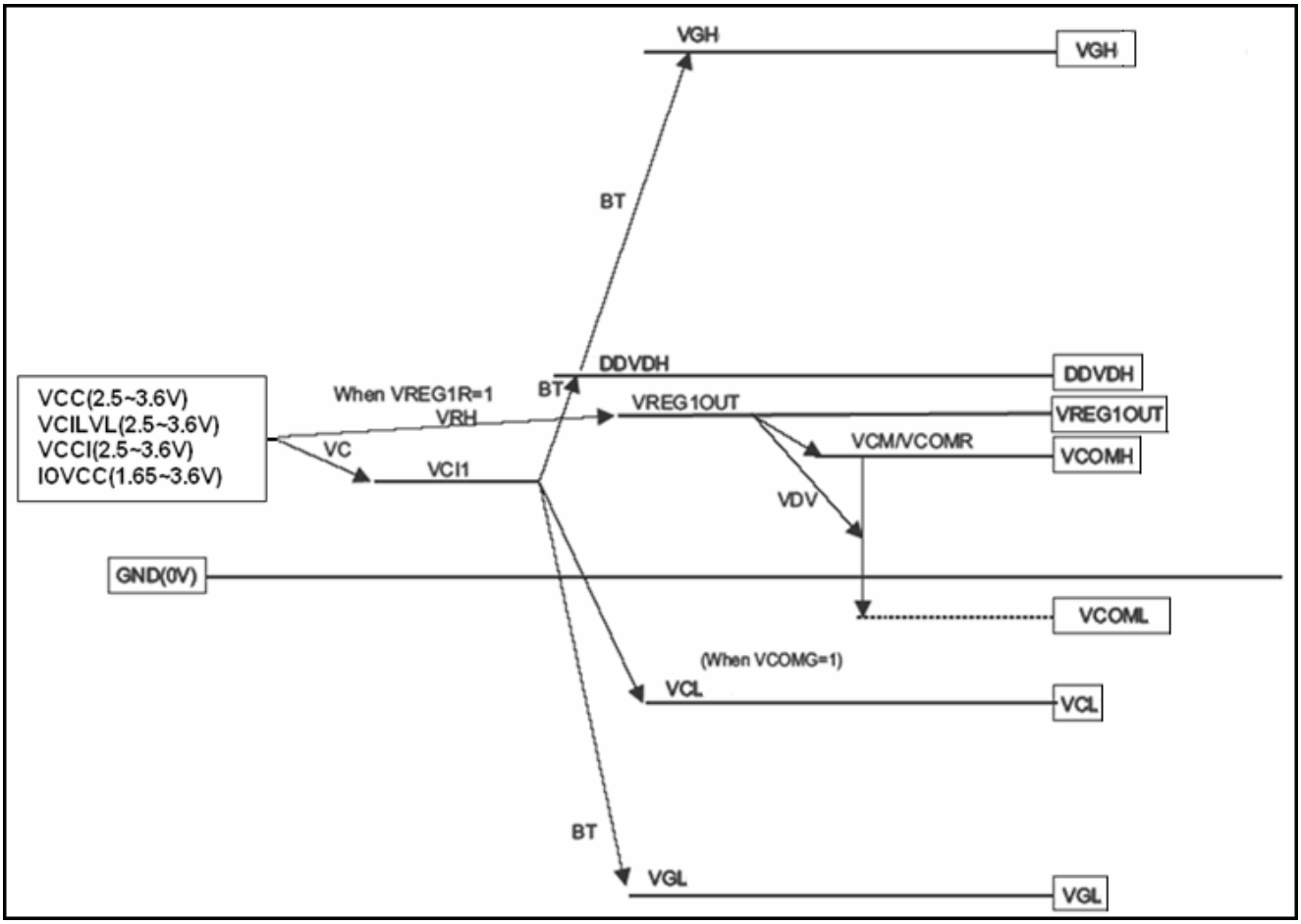
(a) VCI1=VCI direct input



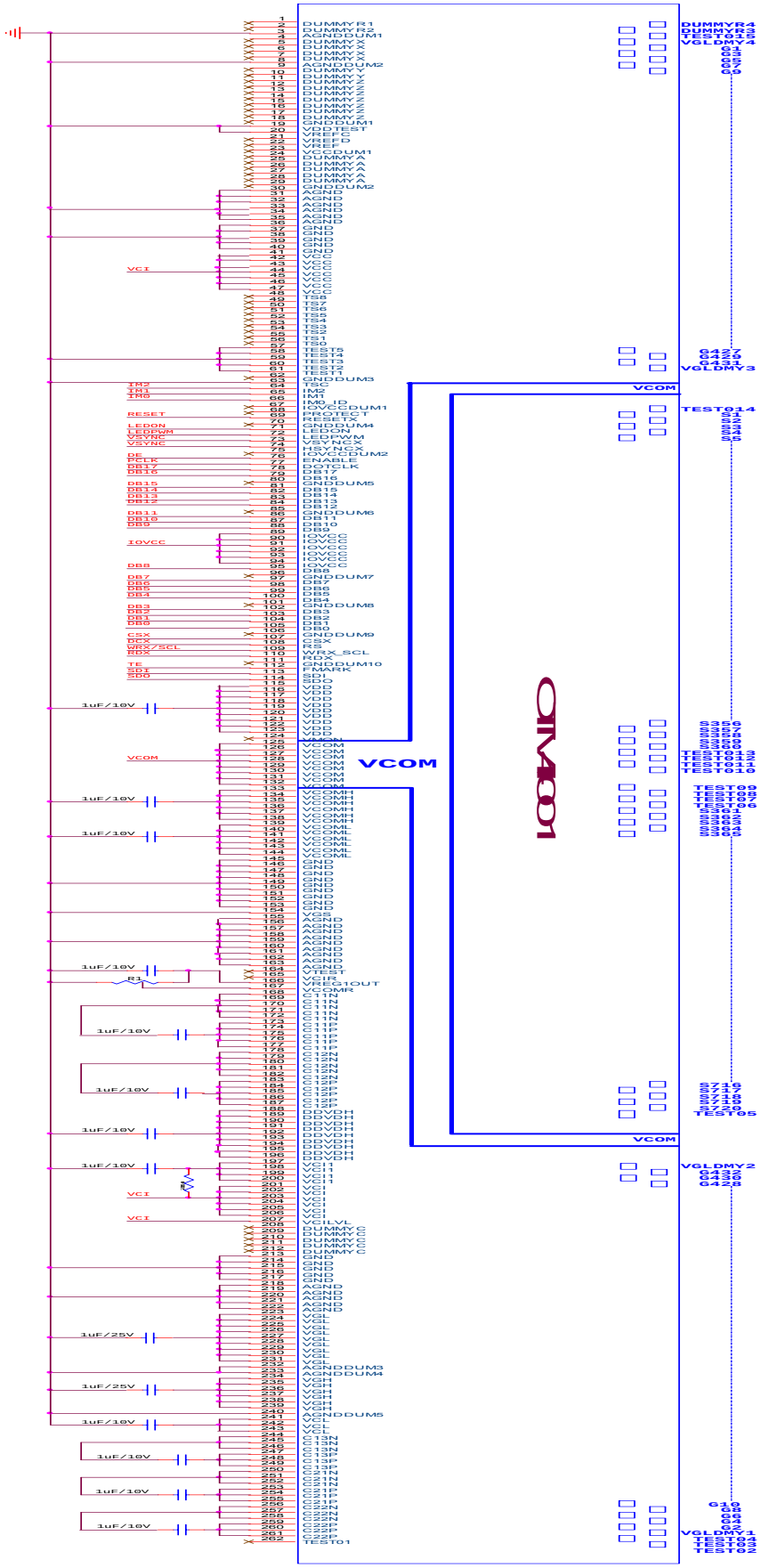
(b) The voltage of **VCI1** Set by **VC2-0**



(c) **Voltage Generation Diagram**



11. Application circuits


VCOM
OTM4001
VCOM
VCOM
VCI
IOVCC
RESET
VSYNC
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
CSX
DCX
WRX/SCL
RDX
TE
SDI
SDO
1uF/10V
1uF/25V
R1

12. Initial Code:

Step	Register Address	Register Value	Note	Step	Register Address	Register Value	Note
1	R0606h	0x0000		44	R0300h	0X0002	
2	Delay 10us			45	R0301h	0X081D	
3	R0007h	0x0001		46	R0302h	0X1621	
4	Delay 10us			47	R0303h	0X3D12	
5	R0110h	0x0001		48	R0304h	0X3C0B	
6	Delay 10us			49	R0305h	0X1004	
7	R0100h	0x17B0		50	R0306h	0X0A06	
8	R0101h	0x0147		51	R0307h	0X0612	
9	R0102h	0x019D		52	R0308h	0X0105	
10	R0103h	0x3600		53	R0309h	0X0004	
11	R0281h	0x0010		54	R030Ah	0X0F05	
12	Delay 10us			55	R030Bh	0X0F00	
13	R0102	0x01BD		56	R030Ch	0X000F	
14	Delay10us			57	R030Dh	0X050F	
14	R0000h	0x0000		58	R030Eh	0X0106	
15	R0001h	0x0000		59	R030Fh	0X0406	
16	R0002h	0x0100		60	R0400h	0X3500	
17	R0003h	0xD090		61	R0401h	0X0001	
18	R0008h	0x0503		62	R0404h	0X0000	
19	R0009h	0x0001		63	R0500h	0X0000	
20	R000Bh	0x0010		64	R0501h	0X0000	
21	R000Ch	0x0000		65	R0502h	0X0000	
22	R000Fh	0x0000		66	R0503h	0X0000	
23	R0007h	0x0001		67	R0504h	0X0000	
24	R0010h	0x0010		68	R0505h	0X0000	
25	R0011h	0x0202		69	R0600h	0X0000	
26	R0012h	0x0300		70	R0606h	0X0000	
27	R0020h	0x021E		71	R06F0h	0X0000	
28	R0021h	0X0202		72	R07F0h	0X5420	
29	R0022h	0X0100		73	R07F2h	0X00DF	
30	R0090h	0X8000		74	R07F3h	0X288A	
31	R0100h	0X16B0		75	R07F4h	0X0022	
32	R0101h	0X0147		76	R07F5h	0X0041	
33	R0102h	0X01BA		77	R07F0h	0X0000	
34	R0103h	0X0600		78	R0007h	0X0173	
35	R0107h	0X0000					
36	R0110h	0X0001					
37	R0210h	0X0000					
38	R0211h	0X00EF					
39	R0212h	0X0000					
40	R0213h	0X01AF					
41	R0280h	0X0000					
42	R0281h	0X0000					
43	R0282h	0X0000					

13. Electrical Characteristics:

13.1. Absolute Maximum Ratings:

Table 13-1

Item	Symbol	Value	Unit	Note
Power Supply Voltage1	VCC,IOVCC	-0.3 ～+4.6	V	
Power Supply Voltage 2	VCI – AGND	-0.3 ～+4.6	V	
Power Supply Voltage 3	DDVDH – AGND	-0.3 ～+6.5	V	
Power Supply Voltage4	AGND – VCL	-0.3 ～+4.6	V	
Power Supply Voltage 5	DDVDH – VCL	-0.3 ～+9.0	V	
Power Supply Voltage7	AGND – VGL	-0.3 ～+14.0	V	
Power Supply Voltage 8	VGH– VGL	-0.3 ～+30.0	V	
Input Voltage	Vt	-0.3 ～IOVCC + 0.3	V	
Operating Temperature	Topr	-40 ～+85	℃	
Storage Temperature	Tstg	-55 ～+110	℃	

13.2. DC Characteristics

Table 13-2 VCC= 2.50V～3.60V, IOVCC=1.65V～ 3.60V, Ta=-40℃～+85℃

Item	Sym bol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	VIH	V	IOVCC=1.65V～3.60V	0.8xIOVCC	-	IOVCC	
Input Low level voltage	VIL	V	IOVCC=1.65V～3.60V	-0.3	-	0.2xIOVCC	
Output ”High” level voltage 1 (DB0-17)	VOH	V	IOVCC=1.65V～3.60V, IOH=-0.1mA	0.8xIOVCC	-	-	
Output ”Low” level voltage 1 (DB0-17)	VOL	V	IOVCC=1.65V～3.60V, IOL=0.1mA	-	-	0.2xIOVCC	
I/O leak current	ILI1	μA	Vin=0～IOVCC1	-1	-	1	
Current Consumption (IOVCC-IOGND)+(VCC-GND) Normal operation mode (262k-colors, display operation)	IOP1	μA	fosc=678kHz (432 line drive), IOVCC=VCC=3.00V fFLM=60Hz Ta=25℃ RAM data: 18’h000000	-	175	-	
Current Consumption (IOVCC-IOGND)+(VCC-GND) 8-color mode, 64-line, partial display operation	Iop2	μA	fosc=376kHz (64-line, partial display), IOVCC=VCC=3.00V, fFLM=40Hz Ta=25℃ RAM data: 18h’000000	-	140	-	

13.3. AC Characteristics

VCC= 2.50V～3.60V，IOVCC=1.65V～3.60V，Ta=-40℃～+85℃

13.3.1. Clock Characteristics

Table 13-3

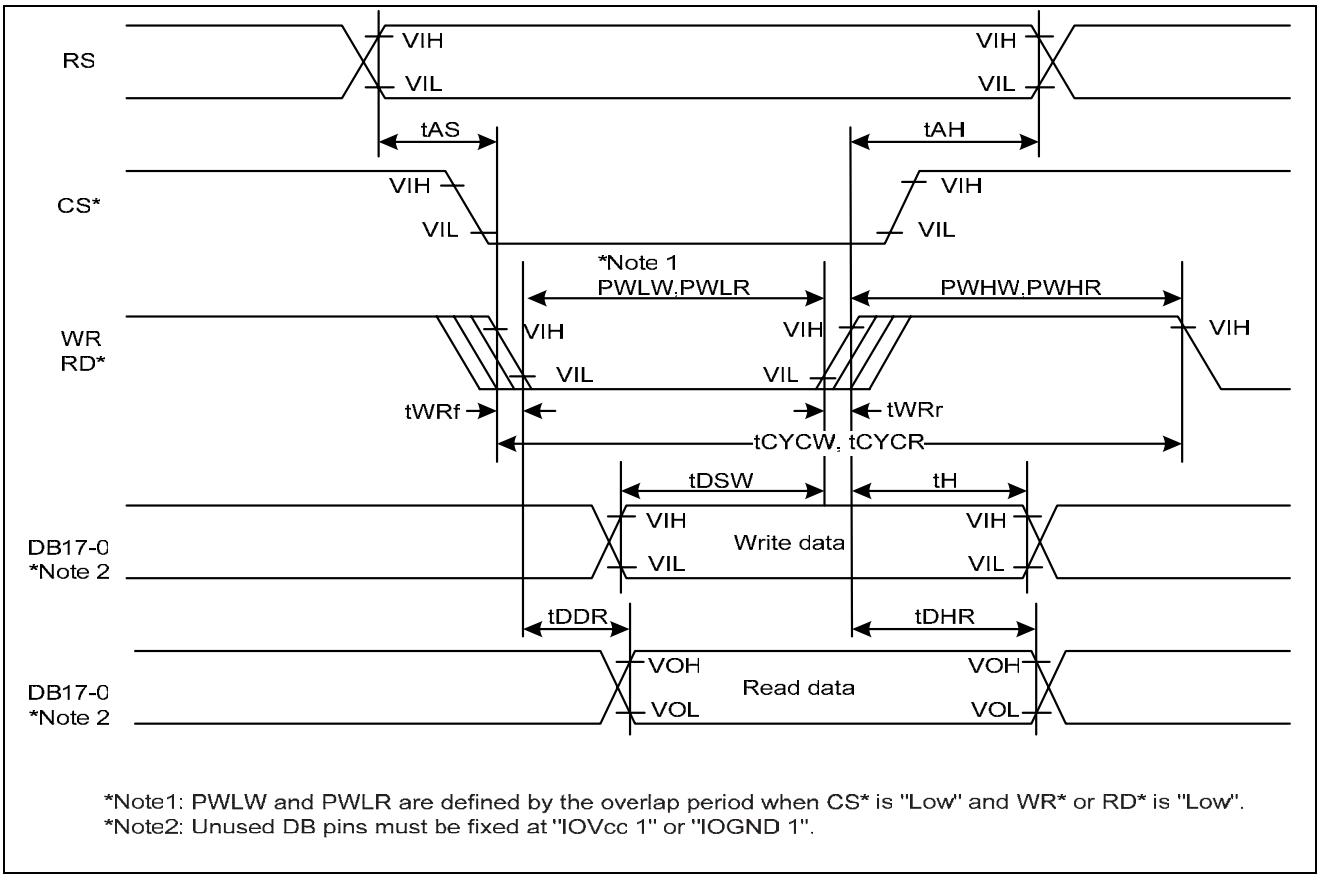
Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	IOVCC = VCC = 3.0V, 25°C	384	427	470	

NOTE：Value of Typ.、Min. and Max. is decided by the setting of Initial Code at Page 61

80-System Bus Interface Timing Characteristics

Table 13-4 Normal write operation (HWM=0), IOVCC=1.65V~3.60V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	150	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	55	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	10
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-



80-System Bus Interface

13.3.2. Clock-synchronized Serial Interface Timing Characteristics

Normal Write Function (HWM=0), High-speed Write Function (HWM=1), IOVCC=1.65~3.60V)

Table 13-5

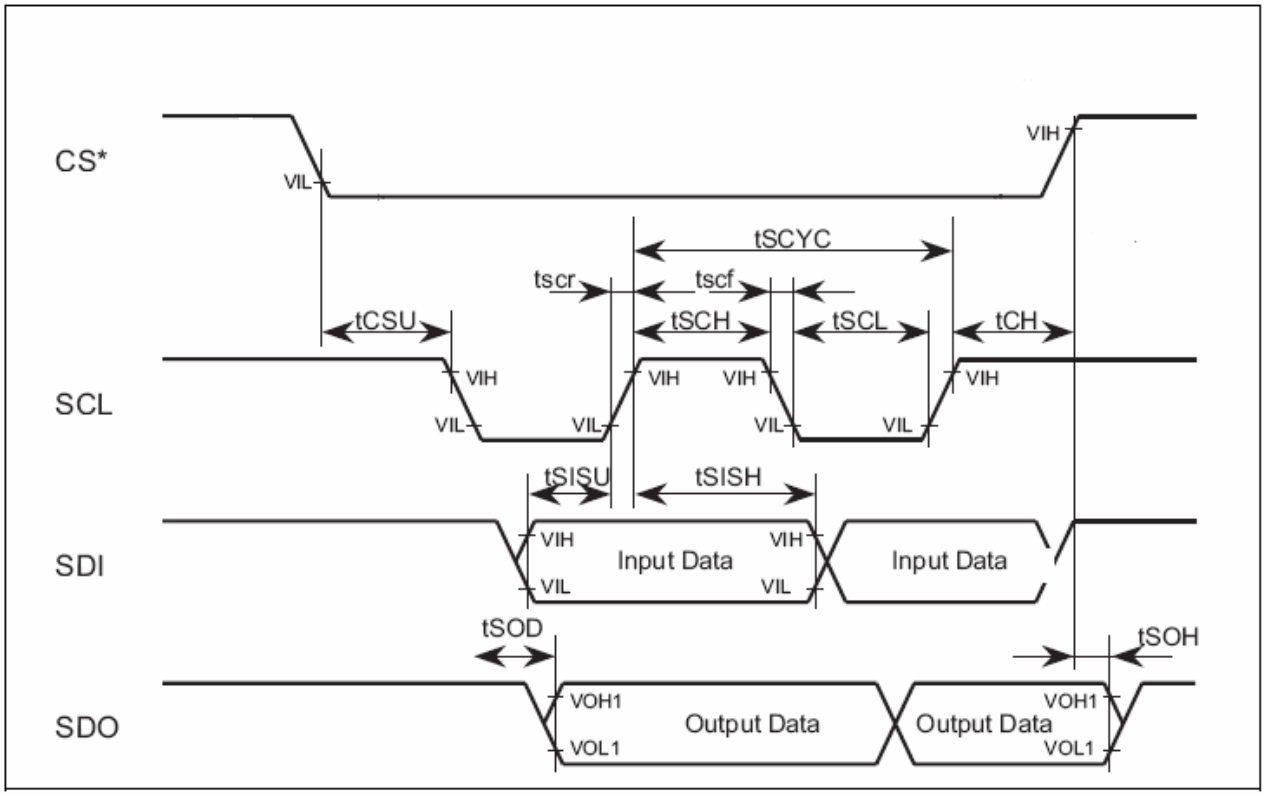
Item	Symbol		Unit	Min.	Typ.	Max.
SerialTime Clock Cycle	Write (received)	tSCYC	ns	100	-	20.000
	Read (transmitted)	tSCYC	ns	350	-	20.000
Serial Clock high-level width	Write (received)	tSCH	ns	40	-	-
	Read (transmitted)	tSCH	ns	150	-	-
Serial Clock low-level width	Write (received)	tSCL	ns	40	-	-
	Read (transmitted)	tSCL	ns	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	60	-	-
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

13.3.3. Reset Timing Characteristics (IOVCC=1.65~3.60V)

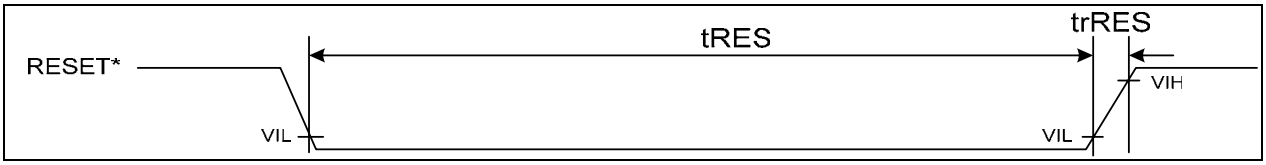
Table 13-6

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—
Reset rise time	trRES	μs	—	—	10

Clock synchronous serial interface



Reset Timing



RGB Interface Timing Characterics

18-/ 16- bit RGB interface (HWM= 1), IOVCC=1.65~3.60V

Table 13-7

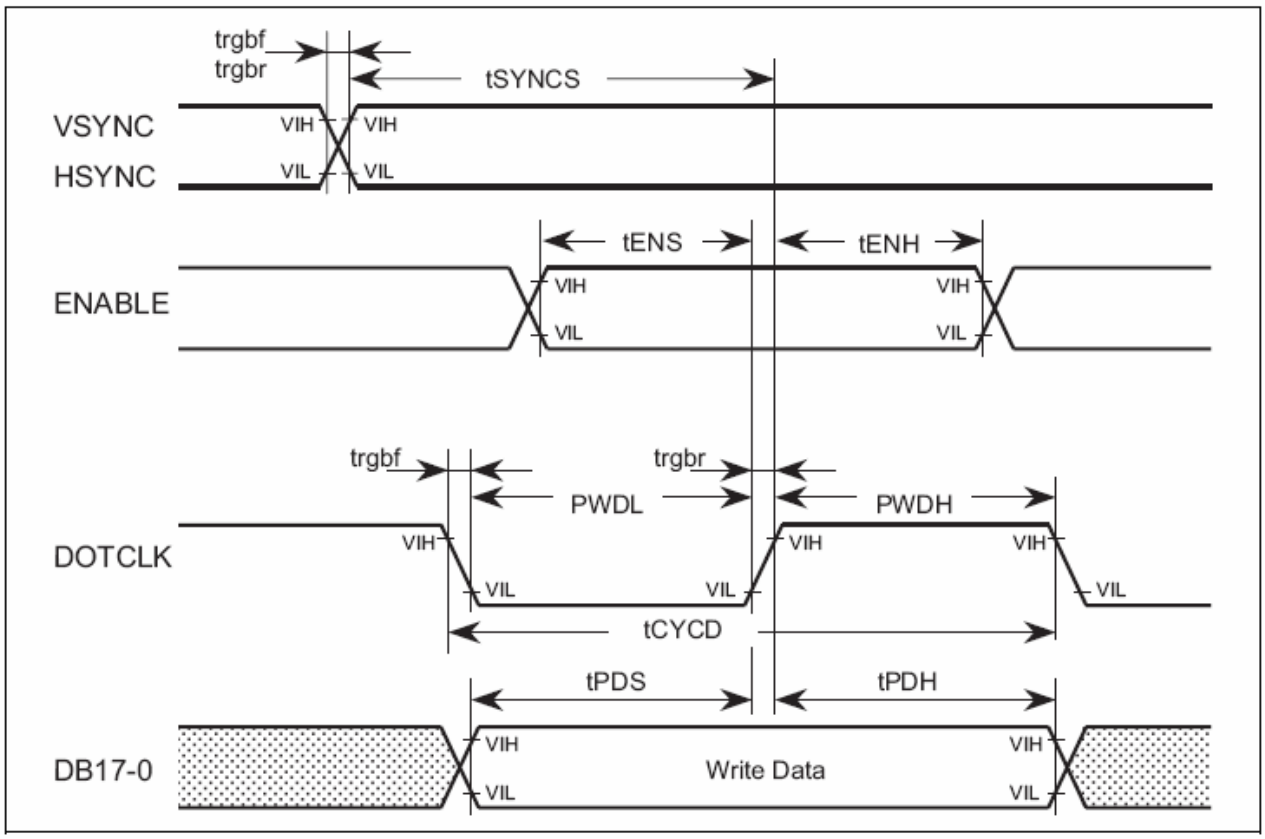
Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	TSYNCS	clock	0	-	1
ENABLE Setup time	TENS	ns	10	-	-
ENABLE Hold time	TENH	ns	20	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	TCYCD	ns	100	-	-
Data setup time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	40	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	Trgbr Trgbf	ns	-	-	25

6-bit RGB interface (HWM = 1), IOVCC=1.65~3.60V

Table 13-8

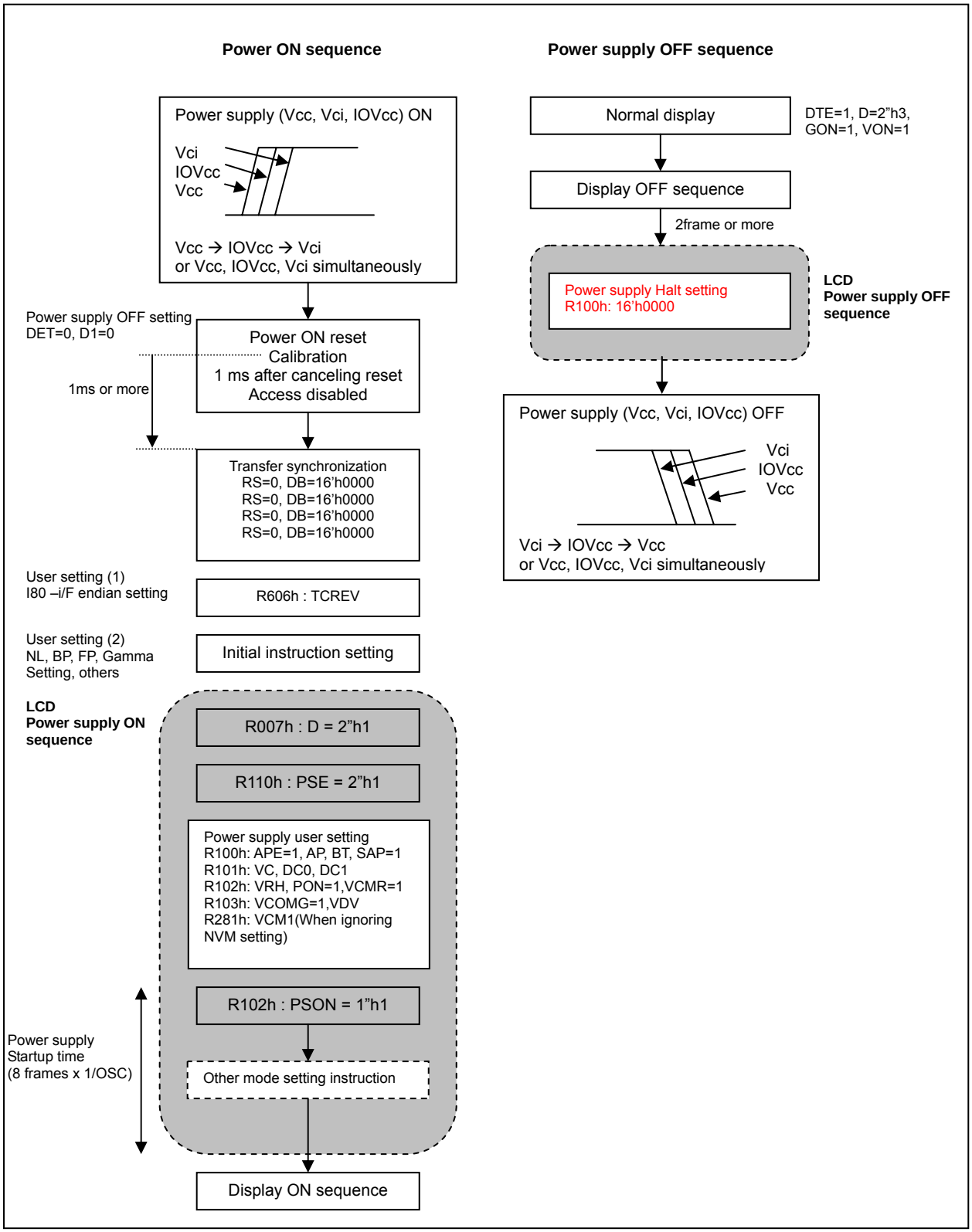
Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	TSYNCS	clock	0	-	1
ENABLE setup time	TENS	ns	10	-	-
ENABLE hold time	TENH	ns	25	-	-
DOTCLK low-level pulse width	PWDL	ns	25	-	-
DOTCLK high-level pulse width	PWDH	ns	25	-	-
DOTCLK cycle time	TCYCD	ns	60	-	-
Data setup-time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	25	-	-
DOTCLK, VSYNC, and HSYNC rise/fall time	Trgb Ttrgbf	ns	-	-	25

RGB Interface



Power On/Off sequence

13.4. Power On / off sequence diagram



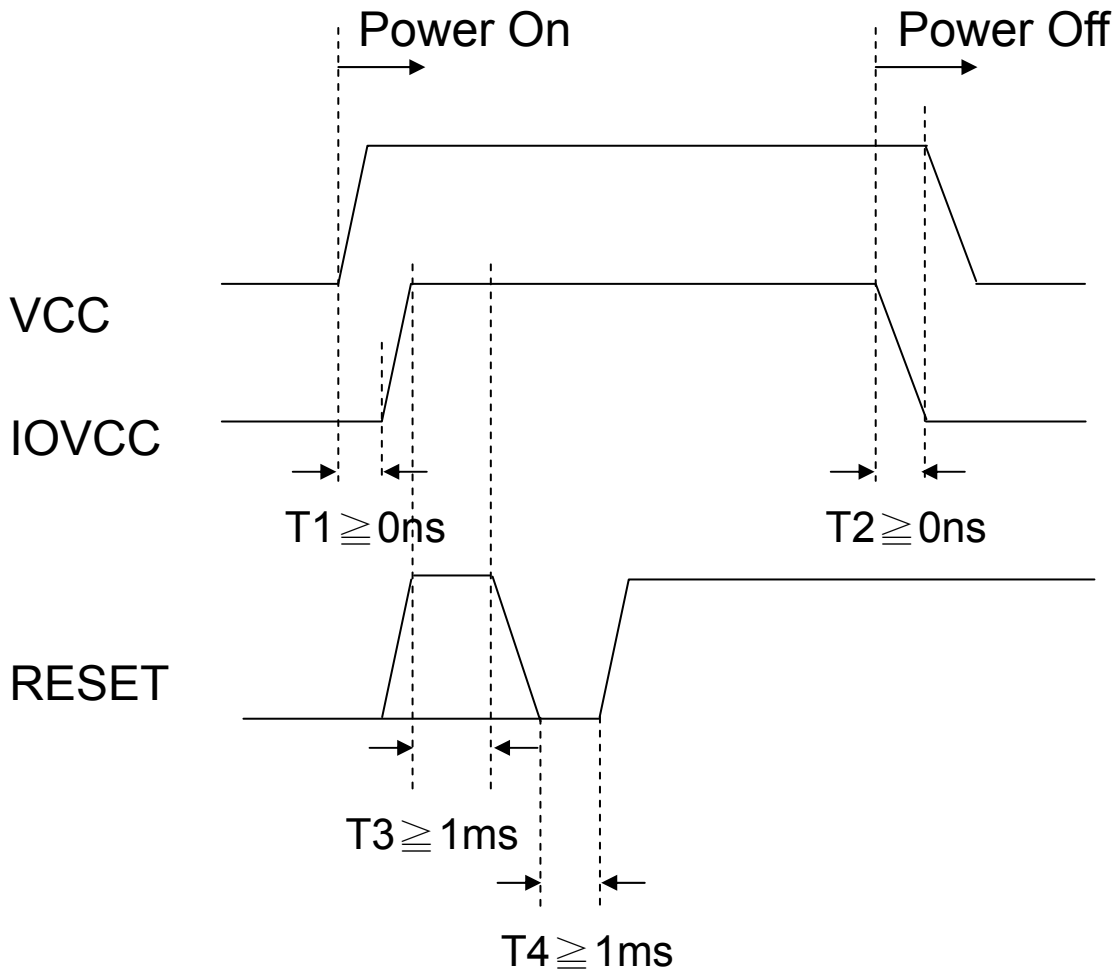
13.5. External-power on/off sequence:

(1) Signal power mode: these three power source VCC, IOVCC and Vci are connected together.

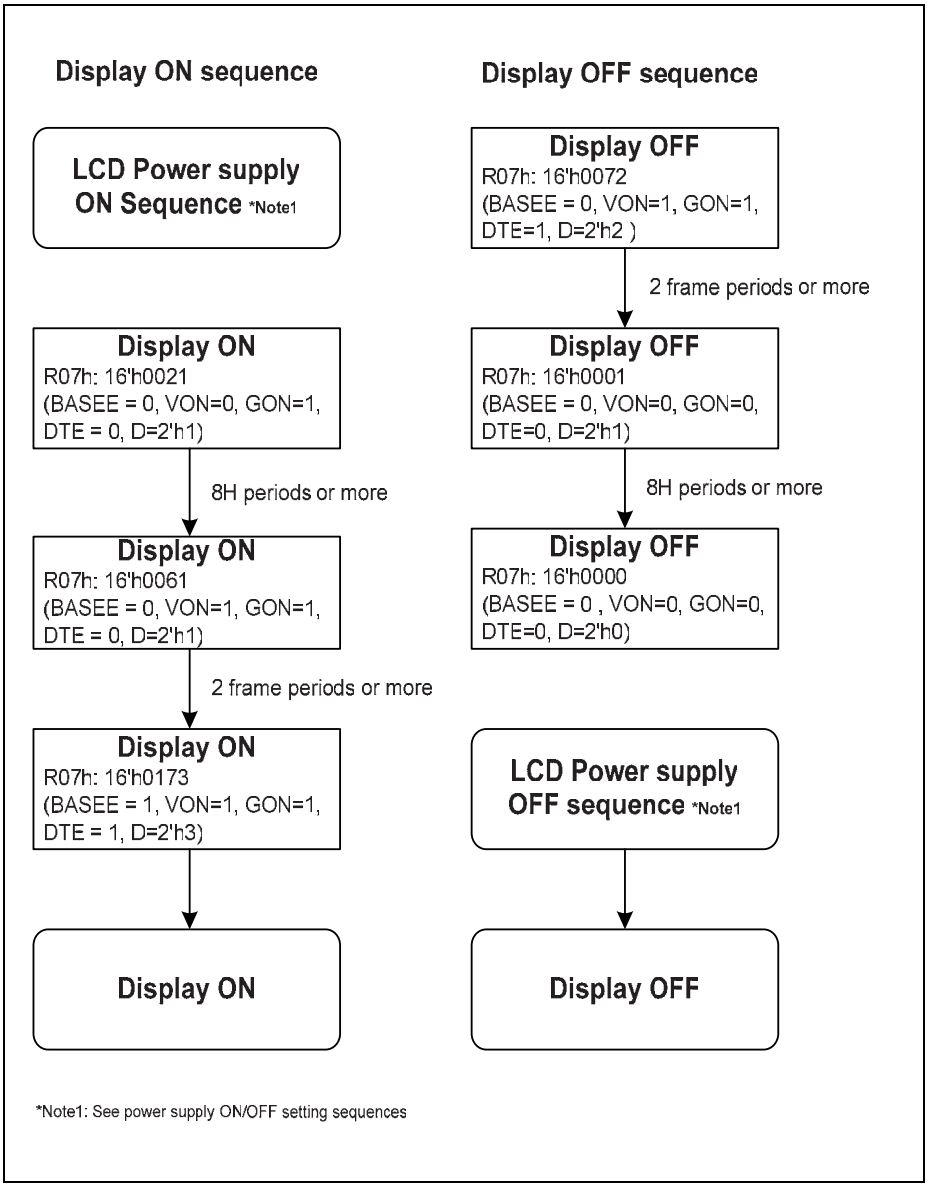
(2) Dual power mode: the two power source VCC and Vci are connected together.

At dual-power mode, VCC power should be earlier turned on than IOVCC, or VCC and VCCIO should be turned on at same time to ensure that a stable state in OTM4001A internal circuit to avoid the wrong logic signal output. When in shutdown, IOVCC power should be earlier turn off than VCC or at the same time in order to avoid the internal logic circuits to give the unknown signal output.

After IOVCC to achieve stable voltage and keep level more than 1ms (T3), the reset low level need keep more than 1ms (T4) to ensure reset function is executed.

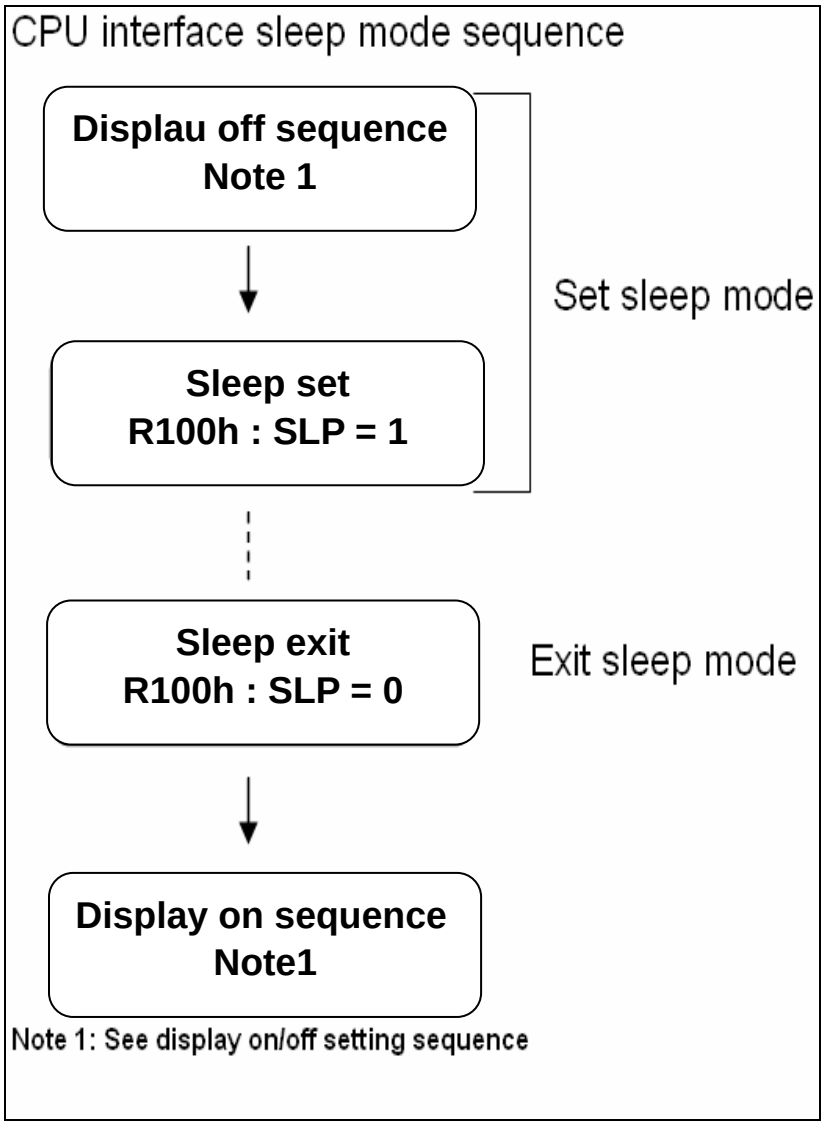


13.6. Display On / Off sequence :

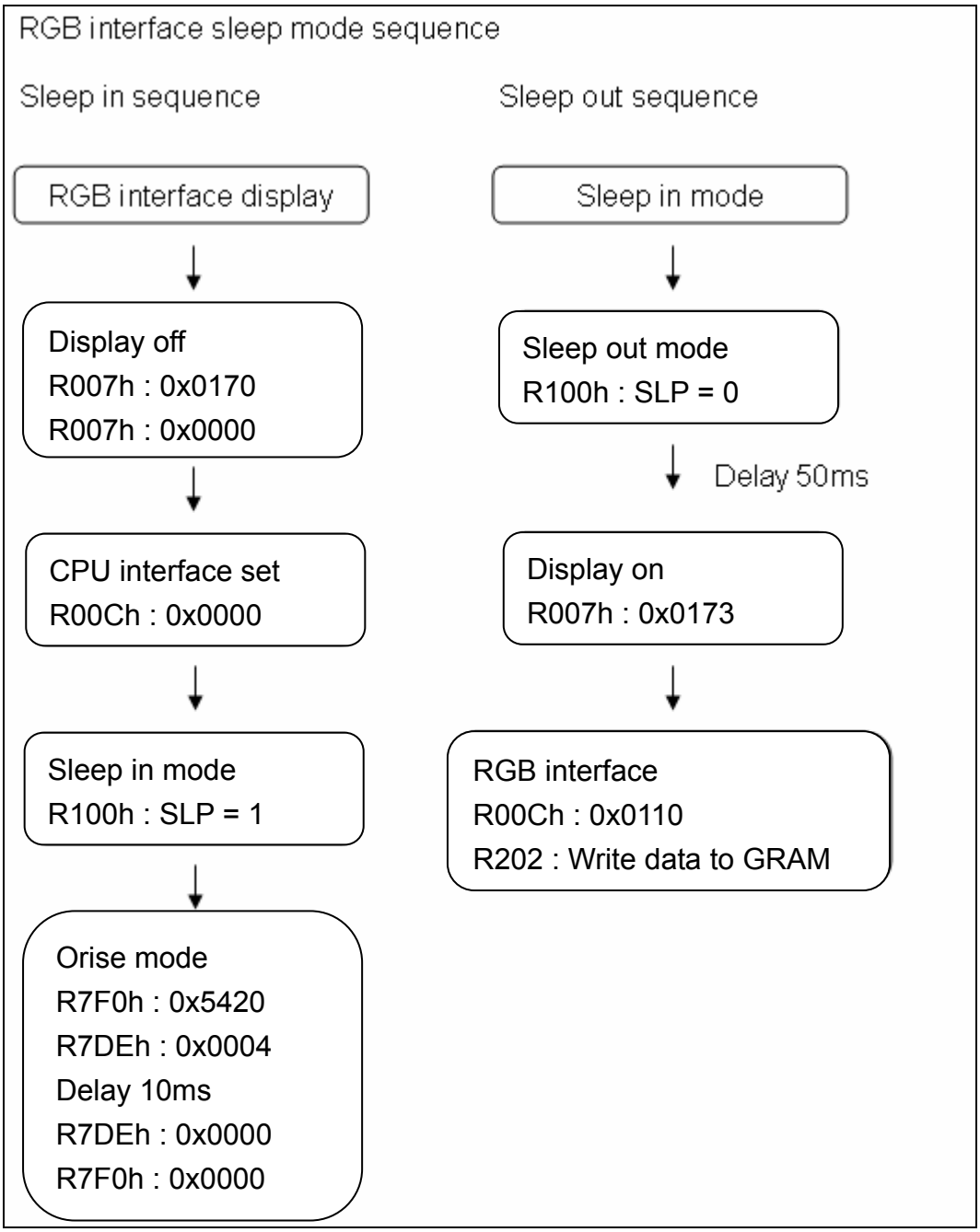


13.7. Sequence to enter and exit sleep mode：

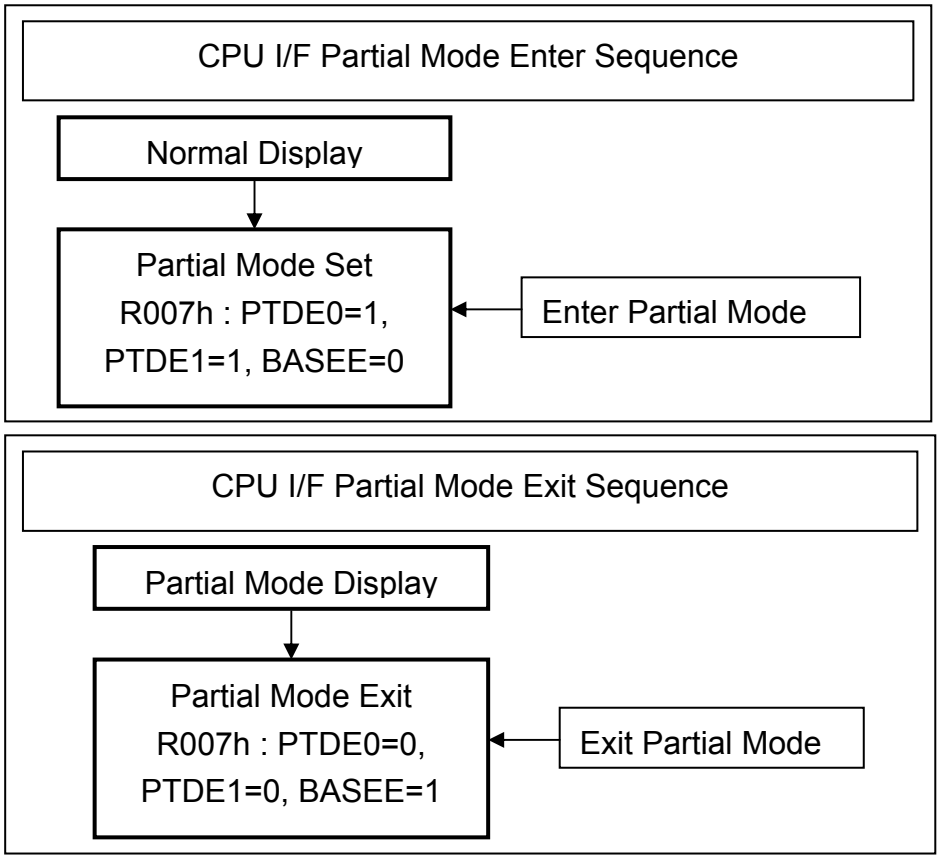
13.7.1. CPU interface mode



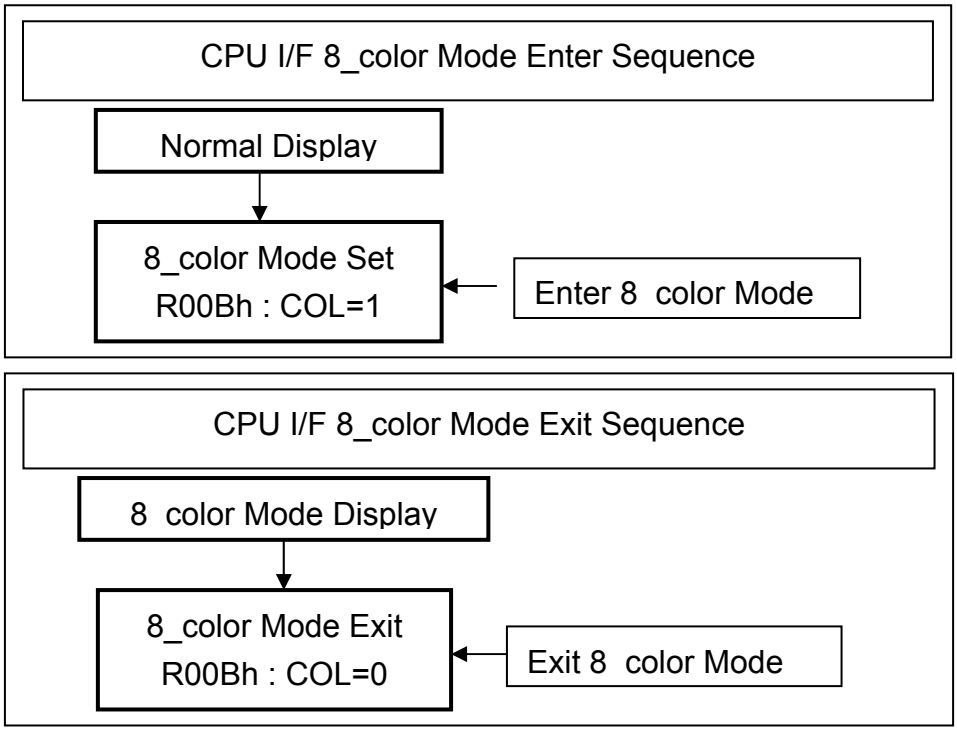
13.7.2. RGB interface mode



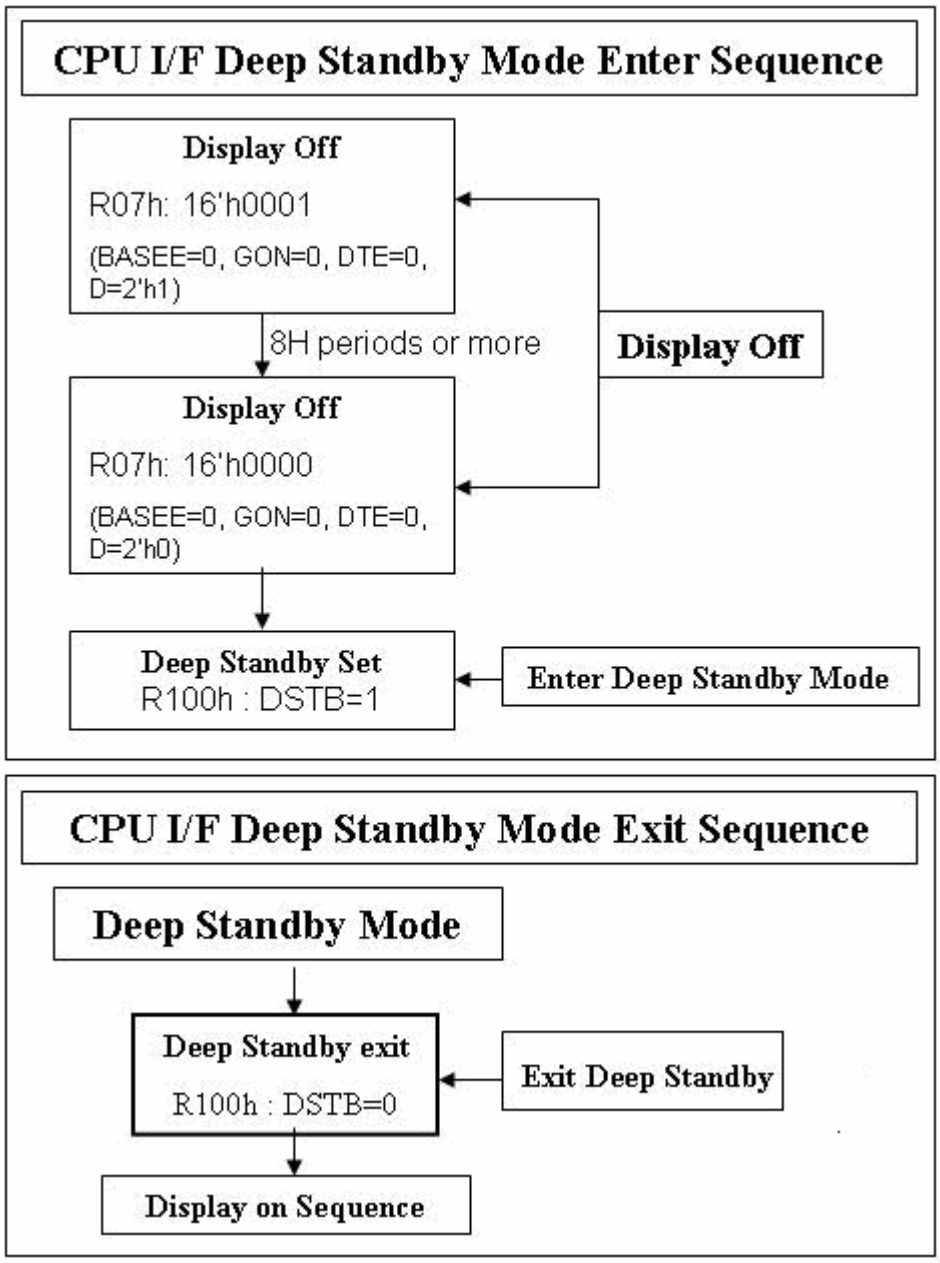
13.8. Partial Display mode



13.9. CPU Interface 8_color mode

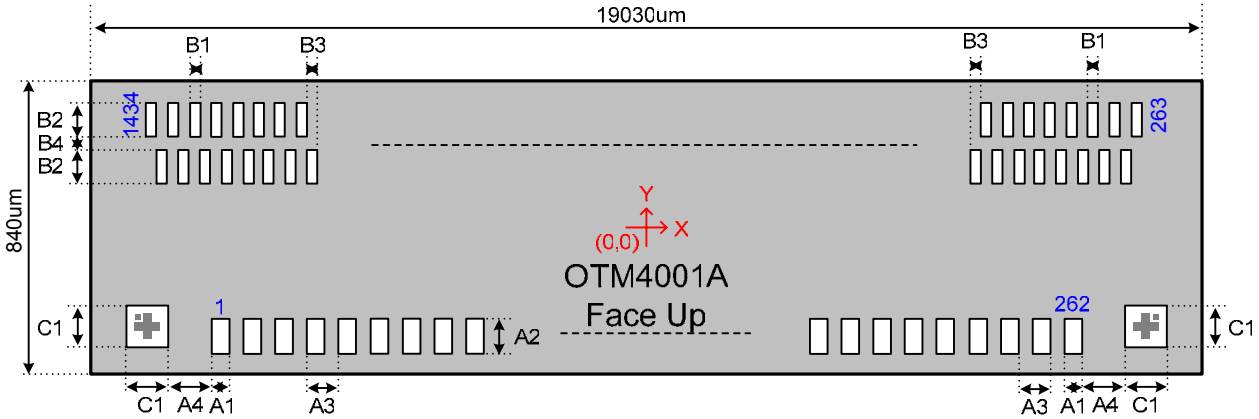


13.10. CPU Interface Deep Standby mode



14. CHIP INFORMATION

14.1. PAD Assignment



Note1: Chip size included scribe line.

Symbol	Size	Symbol	Size	Symbol	Size
A1	50	B1	15	C1	150
A2	90	B2	100	Unit : um	
A3	70	B3	15		
A4	221	B4	19		

14.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	19030	840	μm
Chip thickness	-	400 ± 20 (OTM4001A-C) 280 ± 20 (OTM4001A-C1)		
Pad pitch	1-262	70	-	
	263~1434	15	-	
Pad size	1-262	50	90	
	263-1434	15	100	

Note1: Chip size included scribe line.

14.3. Bump Characteristics

Item	Standard	Note
Bump Hardness	90Hv	± 30Hv
Bump Height	12μm	± 3μm
Co-planarity (in Chip)	R≦ 2μm	R : Max-Min
Roughness (in Bump)	R≦ 2μm	R : Max-Min
Bump Size	Long side ± 2.5μm, short side ± 2μm	
Shear Force	> 5 g/mil^2	

14.4. Pad Locations

NO.	PAD Name	X	Y
1	DUMMYR1	-9135	-289
2	DUMMYR2	-9065	-289
3	AGNDDUM1	-8995	-289
4	DUMMYX	-8925	-289
5	DUMMYX	-8855	-289
6	DUMMYX	-8785	-289
7	DUMMYX	-8715	-289
8	AGNDDUM2	-8645	-289
9	DUMMYY	-8575	-289
10	DUMMYY	-8505	-289
11	DUMMYZ	-8435	-289
12	DUMMYZ	-8365	-289
13	DUMMYZ	-8295	-289
14	DUMMYZ	-8225	-289
15	DUMMYZ	-8155	-289
16	DUMMYZ	-8085	-289
17	DUMMYZ	-8015	-289
18	GNDDUM1	-7945	-289
19	VDDTEST	-7875	-289
20	VREFC	-7805	-289
21	VREFD	-7735	-289
22	VREF	-7665	-289
23	VCCDUM1	-7595	-289
24	DUMMYA	-7525	-289
25	DUMMYA	-7455	-289
26	DUMMYA	-7385	-289
27	DUMMYA	-7315	-289
28	DUMMYA	-7245	-289
29	GNDDUM2	-7175	-289
30	AGND	-7105	-289
31	AGND	-7035	-289
32	AGND	-6965	-289
33	AGND	-6895	-289
34	AGND	-6825	-289
35	AGND	-6755	-289
36	GND	-6685	-289
37	GND	-6615	-289
38	GND	-6545	-289
39	GND	-6475	-289
40	GND	-6405	-289
41	VCC	-6335	-289
42	VCC	-6265	-289
43	VCC	-6195	-289
44	VCC	-6125	-289
45	VCC	-6055	-289
46	VCC	-5985	-289
47	VCC	-5915	-289
48	TS8	-5845	-289
49	TS7	-5775	-289
50	TS6	-5705	-289
51	TS5	-5635	-289
52	TS4	-5565	-289
53	TS3	-5495	-289
54	TS2	-5425	-289
55	TS1	-5355	-289
56	TS0	-5285	-289
57	TEST5	-5215	-289
58	TEST4	-5145	-289
59	TEST3	-5075	-289
60	TEST2	-5005	-289
61	TEST1	-4935	-289
62	GNDDUM3	-4865	-289
63	TSC	-4795	-289
64	IM2	-4725	-289
65	IM1	-4655	-289
66	IM0_ID	-4585	-289
67	IOVCCDUM1	-4515	-289
68	PROTECT	-4445	-289
69	RESETX	-4375	-289
70	GNDDUM4	-4305	-289
71	LEDON	-4235	-289
72	LEDPWM	-4165	-289
73	VSYNCX	-4095	-289
74	HSYNCX	-4025	-289
75	IOVCCDUM2	-3955	-289
76	ENABLE	-3885	-289
77	DOTCLK	-3815	-289
78	DB17	-3745	-289
79	DB16	-3675	-289
80	GNDDUM5	-3605	-289
81	DB15	-3535	-289
82	DB14	-3465	-289
83	DB13	-3395	-289
84	DB12	-3325	-289
85	GNDDUM6	-3255	-289
86	DB11	-3185	-289
87	DB10	-3115	-289
88	DB9	-3045	-289
89	IOVCC	-2975	-289
90	IOVCC	-2905	-289
91	IOVCC	-2835	-289
92	IOVCC	-2765	-289
93	IOVCC	-2695	-289
94	IOVCC	-2625	-289
95	DB8	-2555	-289
96	GNDDUM7	-2485	-289
97	DB7	-2415	-289
98	DB6	-2345	-289
99	DB5	-2275	-289
100	DB4	-2205	-289
101	GNDDUM8	-2135	-289
102	DB3	-2065	-289
103	DB2	-1995	-289
104	DB1	-1925	-289
105	DB0	-1855	-289
106	GNDDUM9	-1785	-289
107	CSX	-1715	-289
108	RS	-1645	-289
109	WRX_SCL	-1575	-289
110	RDX	-1505	-289
111	GNDDUM10	-1435	-289
112	FMARK	-1365	-289
113	SDI	-1295	-289
114	SDO	-1225	-289
115	VDD	-1155	-289
116	VDD	-1085	-289
117	VDD	-1015	-289
118	VDD	-945	-289
119	VDD	-875	-289
120	VDD	-805	-289
121	VDD	-735	-289
122	VDD	-665	-289
123	VDD	-595	-289
124	VMON	-525	-289
125	VCOM	-455	-289
126	VCOM	-385	-289
127	VCOM	-315	-289
128	VCOM	-245	-289
129	VCOM	-175	-289
130	VCOM	-105	-289
131	VCOM	-35	-289
132	VCOM	35	-289
133	VCOMH	105	-289
134	VCOMH	175	-289
135	VCOMH	245	-289
136	VCOMH	315	-289
137	VCOMH	385	-289
138	VCOMH	455	-289
139	VCOML	525	-289
140	VCOML	595	-289
141	VCOML	665	-289
142	VCOML	735	-289
143	VCOML	805	-289
144	VCOML	875	-289
145	GND	945	-289
146	GND	1015	-289
147	GND	1085	-289
148	GND	1155	-289
149	GND	1225	-289
150	GND	1295	-289

NO.	PAD Name	X	Y
151	GND	1365	-289
152	GND	1435	-289
153	GND	1505	-289
154	VGS	1575	-289
155	AGND	1645	-289
156	AGND	1715	-289
157	AGND	1785	-289
158	AGND	1855	-289
159	AGND	1925	-289
160	AGND	1995	-289
161	AGND	2065	-289
162	AGND	2135	-289
163	AGND	2205	-289
164	VTEST	2275	-289
165	VCIR	2345	-289
166	VREG1OUT	2415	-289
167	VCOMR	2485	-289
168	C11N	2555	-289
169	C11N	2625	-289
170	C11N	2695	-289
171	C11N	2765	-289
172	C11N	2835	-289
173	C11P	2905	-289
174	C11P	2975	-289
175	C11P	3045	-289
176	C11P	3115	-289
177	C11P	3185	-289
178	C12N	3255	-289
179	C12N	3325	-289
180	C12N	3395	-289
181	C12N	3465	-289
182	C12N	3535	-289
183	C12P	3605	-289
184	C12P	3675	-289
185	C12P	3745	-289
186	C12P	3815	-289
187	C12P	3885	-289
188	DDVDH	3955	-289
189	DDVDH	4025	-289
190	DDVDH	4095	-289
191	DDVDH	4165	-289
192	DDVDH	4235	-289
193	DDVDH	4305	-289
194	DDVDH	4375	-289
195	DDVDH	4445	-289
196	DDVDH	4515	-289
197	VCI1	4585	-289
198	VCI1	4655	-289
199	VCI1	4725	-289
200	VCI1	4795	-289
201	VCI	4865	-289
202	VCI	4935	-289

NO.	PAD Name	X	Y
203	VCI	5005	-289
204	VCI	5075	-289
205	VCI	5145	-289
206	VCI	5215	-289
207	VCILVL	5285	-289
208	DUMMYC	5355	-289
209	DUMMYC	5425	-289
210	DUMMYC	5495	-289
211	DUMMYC	5565	-289
212	DUMMYC	5635	-289
213	GND	5705	-289
214	GND	5775	-289
215	GND	5845	-289
216	GND	5915	-289
217	GND	5985	-289
218	AGND	6055	-289
219	AGND	6125	-289
220	AGND	6195	-289
221	AGND	6265	-289
222	AGND	6335	-289
223	VGL	6405	-289
224	VGL	6475	-289
225	VGL	6545	-289
226	VGL	6615	-289
227	VGL	6685	-289
228	VGL	6755	-289
229	VGL	6825	-289
230	VGL	6895	-289
231	VGL	6965	-289
232	AGNDDUM3	7035	-289
233	AGNDDUM4	7105	-289
234	VGH	7175	-289
235	VGH	7245	-289
236	VGH	7315	-289
237	VGH	7385	-289
238	VGH	7455	-289
239	VGH	7525	-289
240	AGNDDUM5	7595	-289
241	VCL	7665	-289
242	VCL	7735	-289
243	VCL	7805	-289
244	C13N	7875	-289
245	C13N	7945	-289
246	C13N	8015	-289
247	C13P	8085	-289
248	C13P	8155	-289
249	C13P	8225	-289
250	C21N	8295	-289
251	C21N	8365	-289
252	C21N	8435	-289
253	C21P	8505	-289
254	C21P	8575	-289

NO.	PAD Name	X	Y
255	C21P	8645	-289
256	C22N	8715	-289
257	C22N	8785	-289
258	C22N	8855	-289
259	C22P	8925	-289
260	C22P	8995	-289
261	C22P	9065	-289
262	TESTO1	9135	-289
263	TESTO2	9397.5	177
264	TESTO3	9382.5	296
265	TESTO4	9367.5	177
266	VGLDMY1	9352.5	296
267	G2	9337.5	177
268	G4	9322.5	296
269	G6	9307.5	177
270	G8	9292.5	296
271	G10	9277.5	177
272	G12	9262.5	296
273	G14	9247.5	177
274	G16	9232.5	296
275	G18	9217.5	177
276	G20	9202.5	296
277	G22	9187.5	177
278	G24	9172.5	296
279	G26	9157.5	177
280	G28	9142.5	296
281	G30	9127.5	177
282	G32	9112.5	296
283	G34	9097.5	177
284	G36	9082.5	296
285	G38	9067.5	177
286	G40	9052.5	296
287	G42	9037.5	177
288	G44	9022.5	296
289	G46	9007.5	177
290	G48	8992.5	296
291	G50	8977.5	177
292	G52	8962.5	296
293	G54	8947.5	177
294	G56	8932.5	296
295	G58	8917.5	177
296	G60	8902.5	296
297	G62	8887.5	177
298	G64	8872.5	296
299	G66	8857.5	177
300	G68	8842.5	296
301	G70	8827.5	177
302	G72	8812.5	296
303	G74	8797.5	177
304	G76	8782.5	296
305	G78	8767.5	177
306	G80	8752.5	296

NO.	PAD Name	X	Y
307	G82	8737.5	177
308	G84	8722.5	296
309	G86	8707.5	177
310	G88	8692.5	296
311	G90	8677.5	177
312	G92	8662.5	296
313	G94	8647.5	177
314	G96	8632.5	296
315	G98	8617.5	177
316	G100	8602.5	296
317	G102	8587.5	177
318	G104	8572.5	296
319	G106	8557.5	177
320	G108	8542.5	296
321	G110	8527.5	177
322	G112	8512.5	296
323	G114	8497.5	177
324	G116	8482.5	296
325	G118	8467.5	177
326	G120	8452.5	296
327	G122	8437.5	177
328	G124	8422.5	296
329	G126	8407.5	177
330	G128	8392.5	296
331	G130	8377.5	177
332	G132	8362.5	296
333	G134	8347.5	177
334	G136	8332.5	296
335	G138	8317.5	177
336	G140	8302.5	296
337	G142	8287.5	177
338	G144	8272.5	296
339	G146	8257.5	177
340	G148	8242.5	296
341	G150	8227.5	177
342	G152	8212.5	296
343	G154	8197.5	177
344	G156	8182.5	296
345	G158	8167.5	177
346	G160	8152.5	296
347	G162	8137.5	177
348	G164	8122.5	296
349	G166	8107.5	177
350	G168	8092.5	296
351	G170	8077.5	177
352	G172	8062.5	296
353	G174	8047.5	177
354	G176	8032.5	296
355	G178	8017.5	177
356	G180	8002.5	296
357	G182	7987.5	177
358	G184	7972.5	296
359	G186	7957.5	177
360	G188	7942.5	296
361	G190	7927.5	177
362	G192	7912.5	296
363	G194	7897.5	177
364	G196	7882.5	296
365	G198	7867.5	177
366	G200	7852.5	296
367	G202	7837.5	177
368	G204	7822.5	296
369	G206	7807.5	177
370	G208	7792.5	296
371	G210	7777.5	177
372	G212	7762.5	296
373	G214	7747.5	177
374	G216	7732.5	296
375	G218	7717.5	177
376	G220	7702.5	296
377	G222	7687.5	177
378	G224	7672.5	296
379	G226	7657.5	177
380	G228	7642.5	296
381	G230	7627.5	177
382	G232	7612.5	296
383	G234	7597.5	177
384	G236	7582.5	296
385	G238	7567.5	177
386	G240	7552.5	296
387	G242	7537.5	177
388	G244	7522.5	296
389	G246	7507.5	177
390	G248	7492.5	296
391	G250	7477.5	177
392	G252	7462.5	296
393	G254	7447.5	177
394	G256	7432.5	296
395	G258	7417.5	177
396	G260	7402.5	296
397	G262	7387.5	177
398	G264	7372.5	296
399	G266	7357.5	177
400	G268	7342.5	296
401	G270	7327.5	177
402	G272	7312.5	296
403	G274	7297.5	177
404	G276	7282.5	296
405	G278	7267.5	177
406	G280	7252.5	296
407	G282	7237.5	177
408	G284	7222.5	296
409	G286	7207.5	177
410	G288	7192.5	296
411	G290	7177.5	177
412	G292	7162.5	296
413	G294	7147.5	177
414	G296	7132.5	296
415	G298	7117.5	177
416	G300	7102.5	296
417	G302	7087.5	177
418	G304	7072.5	296
419	G306	7057.5	177
420	G308	7042.5	296
421	G310	7027.5	177
422	G312	7012.5	296
423	G314	6997.5	177
424	G316	6982.5	296
425	G318	6967.5	177
426	G320	6952.5	296
427	G322	6937.5	177
428	G324	6922.5	296
429	G326	6907.5	177
430	G328	6892.5	296
431	G330	6877.5	177
432	G332	6862.5	296
433	G334	6847.5	177
434	G336	6832.5	296
435	G338	6817.5	177
436	G340	6802.5	296
437	G342	6787.5	177
438	G344	6772.5	296
439	G346	6757.5	177
440	G348	6742.5	296
441	G350	6727.5	177
442	G352	6712.5	296
443	G354	6697.5	177
444	G356	6682.5	296
445	G358	6667.5	177
446	G360	6652.5	296
447	G362	6637.5	177
448	G364	6622.5	296
449	G366	6607.5	177
450	G368	6592.5	296
451	G370	6577.5	177
452	G372	6562.5	296
453	G374	6547.5	177
454	G376	6532.5	296
455	G378	6517.5	177
456	G380	6502.5	296
457	G382	6487.5	177
458	G384	6472.5	296
459	G386	6457.5	177
460	G388	6442.5	296
461	G390	6427.5	177
462	G392	6412.5	296

NO.	PAD Name	X	Y
463	G394	6397.5	177
464	G396	6382.5	296
465	G398	6367.5	177
466	G400	6352.5	296
467	G402	6337.5	177
468	G404	6322.5	296
469	G406	6307.5	177
470	G408	6292.5	296
471	G410	6277.5	177
472	G412	6262.5	296
473	G414	6247.5	177
474	G416	6232.5	296
475	G418	6217.5	177
476	G420	6202.5	296
477	G422	6187.5	177
478	G424	6172.5	296
479	G426	6157.5	177
480	G428	6142.5	296
481	G430	6127.5	177
482	G432	6112.5	296
483	VGLDMY2	6097.5	177
484	TESTO5	5887.5	177
485	S720	5872.5	296
486	S719	5857.5	177
487	S718	5842.5	296
488	S717	5827.5	177
489	S716	5812.5	296
490	S715	5797.5	177
491	S714	5782.5	296
492	S713	5767.5	177
493	S712	5752.5	296
494	S711	5737.5	177
495	S710	5722.5	296
496	S709	5707.5	177
497	S708	5692.5	296
498	S707	5677.5	177
499	S706	5662.5	296
500	S705	5647.5	177
501	S704	5632.5	296
502	S703	5617.5	177
503	S702	5602.5	296
504	S701	5587.5	177
505	S700	5572.5	296
506	S699	5557.5	177
507	S698	5542.5	296
508	S697	5527.5	177
509	S696	5512.5	296
510	S695	5497.5	177
511	S694	5482.5	296
512	S693	5467.5	177
513	S692	5452.5	296
514	S691	5437.5	177
515	S690	5422.5	296
516	S689	5407.5	177
517	S688	5392.5	296
518	S687	5377.5	177
519	S686	5362.5	296
520	S685	5347.5	177
521	S684	5332.5	296
522	S683	5317.5	177
523	S682	5302.5	296
524	S681	5287.5	177
525	S680	5272.5	296
526	S679	5257.5	177
527	S678	5242.5	296
528	S677	5227.5	177
529	S676	5212.5	296
530	S675	5197.5	177
531	S674	5182.5	296
532	S673	5167.5	177
533	S672	5152.5	296
534	S671	5137.5	177
535	S670	5122.5	296
536	S669	5107.5	177
537	S668	5092.5	296
538	S667	5077.5	177
539	S666	5062.5	296
540	S665	5047.5	177
541	S664	5032.5	296
542	S663	5017.5	177
543	S662	5002.5	296
544	S661	4987.5	177
545	S660	4972.5	296
546	S659	4957.5	177
547	S658	4942.5	296
548	S657	4927.5	177
549	S656	4912.5	296
550	S655	4897.5	177
551	S654	4882.5	296
552	S653	4867.5	177
553	S652	4852.5	296
554	S651	4837.5	177
555	S650	4822.5	296
556	S649	4807.5	177
557	S648	4792.5	296
558	S647	4777.5	177
559	S646	4762.5	296
560	S645	4747.5	177
561	S644	4732.5	296
562	S643	4717.5	177
563	S642	4702.5	296
564	S641	4687.5	177
565	S640	4672.5	296
566	S639	4657.5	177
567	S638	4642.5	296
568	S637	4627.5	177
569	S636	4612.5	296
570	S635	4597.5	177
571	S634	4582.5	296
572	S633	4567.5	177
573	S632	4552.5	296
574	S631	4537.5	177
575	S630	4522.5	296
576	S629	4507.5	177
577	S628	4492.5	296
578	S627	4477.5	177
579	S626	4462.5	296
580	S625	4447.5	177
581	S624	4432.5	296
582	S623	4417.5	177
583	S622	4402.5	296
584	S621	4387.5	177
585	S620	4372.5	296
586	S619	4357.5	177
587	S618	4342.5	296
588	S617	4327.5	177
589	S616	4312.5	296
590	S615	4297.5	177
591	S614	4282.5	296
592	S613	4267.5	177
593	S612	4252.5	296
594	S611	4237.5	177
595	S610	4222.5	296
596	S609	4207.5	177
597	S608	4192.5	296
598	S607	4177.5	177
599	S606	4162.5	296
600	S605	4147.5	177
601	S604	4132.5	296
602	S603	4117.5	177
603	S602	4102.5	296
604	S601	4087.5	177
605	S600	4072.5	296
606	S599	4057.5	177
607	S598	4042.5	296
608	S597	4027.5	177
609	S596	4012.5	296
610	S595	3997.5	177
611	S594	3982.5	296
612	S593	3967.5	177
613	S592	3952.5	296
614	S591	3937.5	177
615	S590	3922.5	296
616	S589	3907.5	177
617	S588	3892.5	296
618	S587	3877.5	177

NO.	PAD Name	X	Y
619	S586	3862.5	296
620	S585	3847.5	177
621	S584	3832.5	296
622	S583	3817.5	177
623	S582	3802.5	296
624	S581	3787.5	177
625	S580	3772.5	296
626	S579	3757.5	177
627	S578	3742.5	296
628	S577	3727.5	177
629	S576	3712.5	296
630	S575	3697.5	177
631	S574	3682.5	296
632	S573	3667.5	177
633	S572	3652.5	296
634	S571	3637.5	177
635	S570	3622.5	296
636	S569	3607.5	177
637	S568	3592.5	296
638	S567	3577.5	177
639	S566	3562.5	296
640	S565	3547.5	177
641	S564	3532.5	296
642	S563	3517.5	177
643	S562	3502.5	296
644	S561	3487.5	177
645	S560	3472.5	296
646	S559	3457.5	177
647	S558	3442.5	296
648	S557	3427.5	177
649	S556	3412.5	296
650	S555	3397.5	177
651	S554	3382.5	296
652	S553	3367.5	177
653	S552	3352.5	296
654	S551	3337.5	177
655	S550	3322.5	296
656	S549	3307.5	177
657	S548	3292.5	296
658	S547	3277.5	177
659	S546	3262.5	296
660	S545	3247.5	177
661	S544	3232.5	296
662	S543	3217.5	177
663	S542	3202.5	296
664	S541	3187.5	177
665	S540	3172.5	296
666	S539	3157.5	177
667	S538	3142.5	296
668	S537	3127.5	177
669	S536	3112.5	296
670	S535	3097.5	177
671	S534	3082.5	296
672	S533	3067.5	177
673	S532	3052.5	296
674	S531	3037.5	177
675	S530	3022.5	296
676	S529	3007.5	177
677	S528	2992.5	296
678	S527	2977.5	177
679	S526	2962.5	296
680	S525	2947.5	177
681	S524	2932.5	296
682	S523	2917.5	177
683	S522	2902.5	296
684	S521	2887.5	177
685	S520	2872.5	296
686	S519	2857.5	177
687	S518	2842.5	296
688	S517	2827.5	177
689	S516	2812.5	296
690	S515	2797.5	177
691	S514	2782.5	296
692	S513	2767.5	177
693	S512	2752.5	296
694	S511	2737.5	177
695	S510	2722.5	296
696	S509	2707.5	177
697	S508	2692.5	296
698	S507	2677.5	177
699	S506	2662.5	296
700	S505	2647.5	177
701	S504	2632.5	296
702	S503	2617.5	177
703	S502	2602.5	296
704	S501	2587.5	177
705	S500	2572.5	296
706	S499	2557.5	177
707	S498	2542.5	296
708	S497	2527.5	177
709	S496	2512.5	296
710	S495	2497.5	177
711	S494	2482.5	296
712	S493	2467.5	177
713	S492	2452.5	296
714	S491	2437.5	177
715	S490	2422.5	296
716	S489	2407.5	177
717	S488	2392.5	296
718	S487	2377.5	177
719	S486	2362.5	296
720	S485	2347.5	177
721	S484	2332.5	296
722	S483	2317.5	177
723	S482	2302.5	296
724	S481	2287.5	177
725	S480	2272.5	296
726	S479	2257.5	177
727	S478	2242.5	296
728	S477	2227.5	177
729	S476	2212.5	296
730	S475	2197.5	177
731	S474	2182.5	296
732	S473	2167.5	177
733	S472	2152.5	296
734	S471	2137.5	177
735	S470	2122.5	296
736	S469	2107.5	177
737	S468	2092.5	296
738	S467	2077.5	177
739	S466	2062.5	296
740	S465	2047.5	177
741	S464	2032.5	296
742	S463	2017.5	177
743	S462	2002.5	296
744	S461	1987.5	177
745	S460	1972.5	296
746	S459	1957.5	177
747	S458	1942.5	296
748	S457	1927.5	177
749	S456	1912.5	296
750	S455	1897.5	177
751	S454	1882.5	296
752	S453	1867.5	177
753	S452	1852.5	296
754	S451	1837.5	177
755	S450	1822.5	296
756	S449	1807.5	177
757	S448	1792.5	296
758	S447	1777.5	177
759	S446	1762.5	296
760	S445	1747.5	177
761	S444	1732.5	296
762	S443	1717.5	177
763	S442	1702.5	296
764	S441	1687.5	177
765	S440	1672.5	296
766	S439	1657.5	177
767	S438	1642.5	296
768	S437	1627.5	177
769	S436	1612.5	296
770	S435	1597.5	177
771	S434	1582.5	296
772	S433	1567.5	177
773	S432	1552.5	296
774	S431	1537.5	177

NO.	PAD Name	X	Y
775	S430	1522.5	296
776	S429	1507.5	177
777	S428	1492.5	296
778	S427	1477.5	177
779	S426	1462.5	296
780	S425	1447.5	177
781	S424	1432.5	296
782	S423	1417.5	177
783	S422	1402.5	296
784	S421	1387.5	177
785	S420	1372.5	296
786	S419	1357.5	177
787	S418	1342.5	296
788	S417	1327.5	177
789	S416	1312.5	296
790	S415	1297.5	177
791	S414	1282.5	296
792	S413	1267.5	177
793	S412	1252.5	296
794	S411	1237.5	177
795	S410	1222.5	296
796	S409	1207.5	177
797	S408	1192.5	296
798	S407	1177.5	177
799	S406	1162.5	296
800	S405	1147.5	177
801	S404	1132.5	296
802	S403	1117.5	177
803	S402	1102.5	296
804	S401	1087.5	177
805	S400	1072.5	296
806	S399	1057.5	177
807	S398	1042.5	296
808	S397	1027.5	177
809	S396	1012.5	296
810	S395	997.5	177
811	S394	982.5	296
812	S393	967.5	177
813	S392	952.5	296
814	S391	937.5	177
815	S390	922.5	296
816	S389	907.5	177
817	S388	892.5	296
818	S387	877.5	177
819	S386	862.5	296
820	S385	847.5	177
821	S384	832.5	296
822	S383	817.5	177
823	S382	802.5	296
824	S381	787.5	177
825	S380	772.5	296
826	S379	757.5	177
827	S378	742.5	296
828	S377	727.5	177
829	S376	712.5	296
830	S375	697.5	177
831	S374	682.5	296
832	S373	667.5	177
833	S372	652.5	296
834	S371	637.5	177
835	S370	622.5	296
836	S369	607.5	177
837	S368	592.5	296
838	S367	577.5	177
839	S366	562.5	296
840	S365	547.5	177
841	S364	532.5	296
842	S363	517.5	177
843	S362	502.5	296
844	S361	487.5	177
845	TESTO6	472.5	296
846	TESTO7	457.5	177
847	TESTO8	442.5	296
848	TESTO9	427.5	177
849	TESTO10	-427.5	296
850	TESTO11	-442.5	177
851	TESTO12	-457.5	296
852	TESTO13	-472.5	177
853	S360	-487.5	296
854	S359	-502.5	177
855	S358	-517.5	296
856	S357	-532.5	177
857	S356	-547.5	296
858	S355	-562.5	177
859	S354	-577.5	296
860	S353	-592.5	177
861	S352	-607.5	296
862	S351	-622.5	177
863	S350	-637.5	296
864	S349	-652.5	177
865	S348	-667.5	296
866	S347	-682.5	177
867	S346	-697.5	296
868	S345	-712.5	177
869	S344	-727.5	296
870	S343	-742.5	177
871	S342	-757.5	296
872	S341	-772.5	177
873	S340	-787.5	296
874	S339	-802.5	177
875	S338	-817.5	296
876	S337	-832.5	177
877	S336	-847.5	296
878	S335	-862.5	177
879	S334	-877.5	296
880	S333	-892.5	177
881	S332	-907.5	296
882	S331	-922.5	177
883	S330	-937.5	296
884	S329	-952.5	177
885	S328	-967.5	296
886	S327	-982.5	177
887	S326	-997.5	296
888	S325	-1012.5	177
889	S324	-1027.5	296
890	S323	-1042.5	177
891	S322	-1057.5	296
892	S321	-1072.5	177
893	S320	-1087.5	296
894	S319	-1102.5	177
895	S318	-1117.5	296
896	S317	-1132.5	177
897	S316	-1147.5	296
898	S315	-1162.5	177
899	S314	-1177.5	296
900	S313	-1192.5	177
901	S312	-1207.5	296
902	S311	-1222.5	177
903	S310	-1237.5	296
904	S309	-1252.5	177
905	S308	-1267.5	296
906	S307	-1282.5	177
907	S306	-1297.5	296
908	S305	-1312.5	177
909	S304	-1327.5	296
910	S303	-1342.5	177
911	S302	-1357.5	296
912	S301	-1372.5	177
913	S300	-1387.5	296
914	S299	-1402.5	177
915	S298	-1417.5	296
916	S297	-1432.5	177
917	S296	-1447.5	296
918	S295	-1462.5	177
919	S294	-1477.5	296
920	S293	-1492.5	177
921	S292	-1507.5	296
922	S291	-1522.5	177
923	S290	-1537.5	296
924	S289	-1552.5	177
925	S288	-1567.5	296
926	S287	-1582.5	177
927	S286	-1597.5	296
928	S285	-1612.5	177
929	S284	-1627.5	296
930	S283	-1642.5	177

NO.	PAD Name	X	Y
931	S282	-1657.5	296
932	S281	-1672.5	177
933	S280	-1687.5	296
934	S279	-1702.5	177
935	S278	-1717.5	296
936	S277	-1732.5	177
937	S276	-1747.5	296
938	S275	-1762.5	177
939	S274	-1777.5	296
940	S273	-1792.5	177
941	S272	-1807.5	296
942	S271	-1822.5	177
943	S270	-1837.5	296
944	S269	-1852.5	177
945	S268	-1867.5	296
946	S267	-1882.5	177
947	S266	-1897.5	296
948	S265	-1912.5	177
949	S264	-1927.5	296
950	S263	-1942.5	177
951	S262	-1957.5	296
952	S261	-1972.5	177
953	S260	-1987.5	296
954	S259	-2002.5	177
955	S258	-2017.5	296
956	S257	-2032.5	177
957	S256	-2047.5	296
958	S255	-2062.5	177
959	S254	-2077.5	296
960	S253	-2092.5	177
961	S252	-2107.5	296
962	S251	-2122.5	177
963	S250	-2137.5	296
964	S249	-2152.5	177
965	S248	-2167.5	296
966	S247	-2182.5	177
967	S246	-2197.5	296
968	S245	-2212.5	177
969	S244	-2227.5	296
970	S243	-2242.5	177
971	S242	-2257.5	296
972	S241	-2272.5	177
973	S240	-2287.5	296
974	S239	-2302.5	177
975	S238	-2317.5	296
976	S237	-2332.5	177
977	S236	-2347.5	296
978	S235	-2362.5	177
979	S234	-2377.5	296
980	S233	-2392.5	177
981	S232	-2407.5	296
982	S231	-2422.5	177
983	S230	-2437.5	296
984	S229	-2452.5	177
985	S228	-2467.5	296
986	S227	-2482.5	177
987	S226	-2497.5	296
988	S225	-2512.5	177
989	S224	-2527.5	296
990	S223	-2542.5	177
991	S222	-2557.5	296
992	S221	-2572.5	177
993	S220	-2587.5	296
994	S219	-2602.5	177
995	S218	-2617.5	296
996	S217	-2632.5	177
997	S216	-2647.5	296
998	S215	-2662.5	177
999	S214	-2677.5	296
1000	S213	-2692.5	177
1001	S212	-2707.5	296
1002	S211	-2722.5	177
1003	S210	-2737.5	296
1004	S209	-2752.5	177
1005	S208	-2767.5	296
1006	S207	-2782.5	177
1007	S206	-2797.5	296
1008	S205	-2812.5	177
1009	S204	-2827.5	296
1010	S203	-2842.5	177
1011	S202	-2857.5	296
1012	S201	-2872.5	177
1013	S200	-2887.5	296
1014	S199	-2902.5	177
1015	S198	-2917.5	296
1016	S197	-2932.5	177
1017	S196	-2947.5	296
1018	S195	-2962.5	177
1019	S194	-2977.5	296
1020	S193	-2992.5	177
1021	S192	-3007.5	296
1022	S191	-3022.5	177
1023	S190	-3037.5	296
1024	S189	-3052.5	177
1025	S188	-3067.5	296
1026	S187	-3082.5	177
1027	S186	-3097.5	296
1028	S185	-3112.5	177
1029	S184	-3127.5	296
1030	S183	-3142.5	177
1031	S182	-3157.5	296
1032	S181	-3172.5	177
1033	S180	-3187.5	296
1034	S179	-3202.5	177
1035	S178	-3217.5	296
1036	S177	-3232.5	177
1037	S176	-3247.5	296
1038	S175	-3262.5	177
1039	S174	-3277.5	296
1040	S173	-3292.5	177
1041	S172	-3307.5	296
1042	S171	-3322.5	177
1043	S170	-3337.5	296
1044	S169	-3352.5	177
1045	S168	-3367.5	296
1046	S167	-3382.5	177
1047	S166	-3397.5	296
1048	S165	-3412.5	177
1049	S164	-3427.5	296
1050	S163	-3442.5	177
1051	S162	-3457.5	296
1052	S161	-3472.5	177
1053	S160	-3487.5	296
1054	S159	-3502.5	177
1055	S158	-3517.5	296
1056	S157	-3532.5	177
1057	S156	-3547.5	296
1058	S155	-3562.5	177
1059	S154	-3577.5	296
1060	S153	-3592.5	177
1061	S152	-3607.5	296
1062	S151	-3622.5	177
1063	S150	-3637.5	296
1064	S149	-3652.5	177
1065	S148	-3667.5	296
1066	S147	-3682.5	177
1067	S146	-3697.5	296
1068	S145	-3712.5	177
1069	S144	-3727.5	296
1070	S143	-3742.5	177
1071	S142	-3757.5	296
1072	S141	-3772.5	177
1073	S140	-3787.5	296
1074	S139	-3802.5	177
1075	S138	-3817.5	296
1076	S137	-3832.5	177
1077	S136	-3847.5	296
1078	S135	-3862.5	177
1079	S134	-3877.5	296
1080	S133	-3892.5	177
1081	S132	-3907.5	296
1082	S131	-3922.5	177
1083	S130	-3937.5	296
1084	S129	-3952.5	177
1085	S128	-3967.5	296
1086	S127	-3982.5	177

NO.	PAD Name	X	Y
1087	S126	-3997.5	296
1088	S125	-4012.5	177
1089	S124	-4027.5	296
1090	S123	-4042.5	177
1091	S122	-4057.5	296
1092	S121	-4072.5	177
1093	S120	-4087.5	296
1094	S119	-4102.5	177
1095	S118	-4117.5	296
1096	S117	-4132.5	177
1097	S116	-4147.5	296
1098	S115	-4162.5	177
1099	S114	-4177.5	296
1100	S113	-4192.5	177
1101	S112	-4207.5	296
1102	S111	-4222.5	177
1103	S110	-4237.5	296
1104	S109	-4252.5	177
1105	S108	-4267.5	296
1106	S107	-4282.5	177
1107	S106	-4297.5	296
1108	S105	-4312.5	177
1109	S104	-4327.5	296
1110	S103	-4342.5	177
1111	S102	-4357.5	296
1112	S101	-4372.5	177
1113	S100	-4387.5	296
1114	S99	-4402.5	177
1115	S98	-4417.5	296
1116	S97	-4432.5	177
1117	S96	-4447.5	296
1118	S95	-4462.5	177
1119	S94	-4477.5	296
1120	S93	-4492.5	177
1121	S92	-4507.5	296
1122	S91	-4522.5	177
1123	S90	-4537.5	296
1124	S89	-4552.5	177
1125	S88	-4567.5	296
1126	S87	-4582.5	177
1127	S86	-4597.5	296
1128	S85	-4612.5	177
1129	S84	-4627.5	296
1130	S83	-4642.5	177
1131	S82	-4657.5	296
1132	S81	-4672.5	177
1133	S80	-4687.5	296
1134	S79	-4702.5	177
1135	S78	-4717.5	296
1136	S77	-4732.5	177
1137	S76	-4747.5	296
1138	S75	-4762.5	177
1139	S74	-4777.5	296
1140	S73	-4792.5	177
1141	S72	-4807.5	296
1142	S71	-4822.5	177
1143	S70	-4837.5	296
1144	S69	-4852.5	177
1145	S68	-4867.5	296
1146	S67	-4882.5	177
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1150	S63	-4942.5	177
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1152	S61	-4972.5	177
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1155	S58	-5017.5	296
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1158	S55	-5062.5	177
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1160	S53	-5092.5	177
1161	S52	-5107.5	296
1162	S51	-5122.5	177
1163	S50	-5137.5	296
1164	S49	-5152.5	177
1165	S48	-5167.5	296
1166	S47	-5182.5	177
1167	S46	-5197.5	296
1168	S45	-5212.5	177
1169	S44	-5227.5	296
1170	S43	-5242.5	177
1171	S42	-5257.5	296
1172	S41	-5272.5	177
1173	S40	-5287.5	296
1174	S39	-5302.5	177
1175	S38	-5317.5	296
1176	S37	-5332.5	177
1177	S36	-5347.5	296
1178	S35	-5362.5	177
1179	S34	-5377.5	296
1180	S33	-5392.5	177
1181	S32	-5407.5	296
1182	S31	-5422.5	177
1183	S30	-5437.5	296
1184	S29	-5452.5	177
1185	S28	-5467.5	296
1186	S27	-5482.5	177
1187	S26	-5497.5	296
1188	S25	-5512.5	177
1189	S24	-5527.5	296
1190	S23	-5542.5	177
1191	S22	-5557.5	296
1192	S21	-5572.5	177
1193	S20	-5587.5	296
1194	S19	-5602.5	177
1195	S18	-5617.5	296
1196	S17	-5632.5	177
1197	S16	-5647.5	296
1198	S15	-5662.5	177
1199	S14	-5677.5	296
1200	S13	-5692.5	177
1201	S12	-5707.5	296
1202	S11	-5722.5	177
1203	S10	-5737.5	296
1204	S9	-5752.5	177
1205	S8	-5767.5	296
1206	S7	-5782.5	177
1207	S6	-5797.5	296
1208	S5	-5812.5	177
1209	S4	-5827.5	296
1210	S3	-5842.5	177
1211	S2	-5857.5	296
1212	S1	-5872.5	177
1213	TESTO14	-5887.5	296
1214	VGLDMY3	-6097.5	296
1215	G431	-6112.5	177
1216	G429	-6127.5	296
1217	G427	-6142.5	177
1218	G425	-6157.5	296
1219	G423	-6172.5	177
1220	G421	-6187.5	296
1221	G419	-6202.5	177
1222	G417	-6217.5	296
1223	G415	-6232.5	177
1224	G413	-6247.5	296
1225	G411	-6262.5	177
1226	G409	-6277.5	296
1227	G407	-6292.5	177
1228	G405	-6307.5	296
1229	G403	-6322.5	177
1230	G401	-6337.5	296
1231	G399	-6352.5	177
1232	G397	-6367.5	296
1233	G395	-6382.5	177
1234	G393	-6397.5	296
1235	G391	-6412.5	177
1236	G389	-6427.5	296
1237	G387	-6442.5	177
1238	G385	-6457.5	296
1239	G383	-6472.5	177
1240	G381	-6487.5	296
1241	G379	-6502.5	177
1242	G377	-6517.5	296

NO.	PAD Name	X	Y
1243	G375	-6532.5	177
1244	G373	-6547.5	296
1245	G371	-6562.5	177
1246	G369	-6577.5	296
1247	G367	-6592.5	177
1248	G365	-6607.5	296
1249	G363	-6622.5	177
1250	G361	-6637.5	296
1251	G359	-6652.5	177
1252	G357	-6667.5	296
1253	G355	-6682.5	177
1254	G353	-6697.5	296
1255	G351	-6712.5	177
1256	G349	-6727.5	296
1257	G347	-6742.5	177
1258	G345	-6757.5	296
1259	G343	-6772.5	177
1260	G341	-6787.5	296
1261	G339	-6802.5	177
1262	G337	-6817.5	296
1263	G335	-6832.5	177
1264	G333	-6847.5	296
1265	G331	-6862.5	177
1266	G329	-6877.5	296
1267	G327	-6892.5	177
1268	G325	-6907.5	296
1269	G323	-6922.5	177
1270	G321	-6937.5	296
1271	G319	-6952.5	177
1272	G317	-6967.5	296
1273	G315	-6982.5	177
1274	G313	-6997.5	296
1275	G311	-7012.5	177
1276	G309	-7027.5	296
1277	G307	-7042.5	177
1278	G305	-7057.5	296
1279	G303	-7072.5	177
1280	G301	-7087.5	296
1281	G299	-7102.5	177
1282	G297	-7117.5	296
1283	G295	-7132.5	177
1284	G293	-7147.5	296
1285	G291	-7162.5	177
1286	G289	-7177.5	296
1287	G287	-7192.5	177
1288	G285	-7207.5	296
1289	G283	-7222.5	177
1290	G281	-7237.5	296
1291	G279	-7252.5	177
1292	G277	-7267.5	296
1293	G275	-7282.5	177
1294	G273	-7297.5	296
1295	G271	-7312.5	177
1296	G269	-7327.5	296
1297	G267	-7342.5	177
1298	G265	-7357.5	296
1299	G263	-7372.5	177
1300	G261	-7387.5	296
1301	G259	-7402.5	177
1302	G257	-7417.5	296
1303	G255	-7432.5	177
1304	G253	-7447.5	296
1305	G251	-7462.5	177
1306	G249	-7477.5	296
1307	G247	-7492.5	177
1308	G245	-7507.5	296
1309	G243	-7522.5	177
1310	G241	-7537.5	296
1311	G239	-7552.5	177
1312	G237	-7567.5	296
1313	G235	-7582.5	177
1314	G233	-7597.5	296
1315	G231	-7612.5	177
1316	G229	-7627.5	296
1317	G227	-7642.5	177
1318	G225	-7657.5	296
1319	G223	-7672.5	177
1320	G221	-7687.5	296
1321	G219	-7702.5	177
1322	G217	-7717.5	296
1323	G215	-7732.5	177
1324	G213	-7747.5	296
1325	G211	-7762.5	177
1326	G209	-7777.5	296
1327	G207	-7792.5	177
1328	G205	-7807.5	296
1329	G203	-7822.5	177
1330	G201	-7837.5	296
1331	G199	-7852.5	177
1332	G197	-7867.5	296
1333	G195	-7882.5	177
1334	G193	-7897.5	296
1335	G191	-7912.5	177
1336	G189	-7927.5	296
1337	G187	-7942.5	177
1338	G185	-7957.5	296
1339	G183	-7972.5	177
1340	G181	-7987.5	296
1341	G179	-8002.5	177
1342	G177	-8017.5	296
1343	G175	-8032.5	177
1344	G173	-8047.5	296
1345	G171	-8062.5	177
1346	G169	-8077.5	296
1347	G167	-8092.5	177
1348	G165	-8107.5	296
1349	G163	-8122.5	177
1350	G161	-8137.5	296
1351	G159	-8152.5	177
1352	G157	-8167.5	296
1353	G155	-8182.5	177
1354	G153	-8197.5	296
1355	G151	-8212.5	177
1356	G149	-8227.5	296
1357	G147	-8242.5	177
1358	G145	-8257.5	296
1359	G143	-8272.5	177
1360	G141	-8287.5	296
1361	G139	-8302.5	177
1362	G137	-8317.5	296
1363	G135	-8332.5	177
1364	G133	-8347.5	296
1365	G131	-8362.5	177
1366	G129	-8377.5	296
1367	G127	-8392.5	177
1368	G125	-8407.5	296
1369	G123	-8422.5	177
1370	G121	-8437.5	296
1371	G119	-8452.5	177
1372	G117	-8467.5	296
1373	G115	-8482.5	177
1374	G113	-8497.5	296
1375	G111	-8512.5	177
1376	G109	-8527.5	296
1377	G107	-8542.5	177
1378	G105	-8557.5	296
1379	G103	-8572.5	177
1380	G101	-8587.5	296
1381	G99	-8602.5	177
1382	G97	-8617.5	296
1383	G95	-8632.5	177
1384	G93	-8647.5	296
1385	G91	-8662.5	177
1386	G89	-8677.5	296
1387	G87	-8692.5	177
1388	G85	-8707.5	296
1389	G83	-8722.5	177
1390	G81	-8737.5	296
1391	G79	-8752.5	177
1392	G77	-8767.5	296
1393	G75	-8782.5	177
1394	G73	-8797.5	296
1395	G71	-8812.5	177
1396	G69	-8827.5	296
1397	G67	-8842.5	177
1398	G65	-8857.5	296

NO.	PAD Name	X	Y
1399	G63	-8872.5	177
1400	G61	-8887.5	296
1401	G59	-8902.5	177
1402	G57	-8917.5	296
1403	G55	-8932.5	177
1404	G53	-8947.5	296
1405	G51	-8962.5	177
1406	G49	-8977.5	296
1407	G47	-8992.5	177
1408	G45	-9007.5	296
1409	G43	-9022.5	177
1410	G41	-9037.5	296
1411	G39	-9052.5	177

NO.	PAD Name	X	Y
1412	G37	-9067.5	296
1413	G35	-9082.5	177
1414	G33	-9097.5	296
1415	G31	-9112.5	177
1416	G29	-9127.5	296
1417	G27	-9142.5	177
1418	G25	-9157.5	296
1419	G23	-9172.5	177
1420	G21	-9187.5	296
1421	G19	-9202.5	177
1422	G17	-9217.5	296
1423	G15	-9232.5	177
1424	G13	-9247.5	296

NO.	PAD Name	X	Y
1425	G11	-9262.5	177
1426	G9	-9277.5	296
1427	G7	-9292.5	177
1428	G5	-9307.5	296
1429	G3	-9322.5	177
1430	G1	-9337.5	296
1431	VGLDMY4	-9352.5	177
1432	TESTO15	-9367.5	296
1433	DUMMYR3	-9382.5	177
1434	DUMMYR4	-9397.5	296

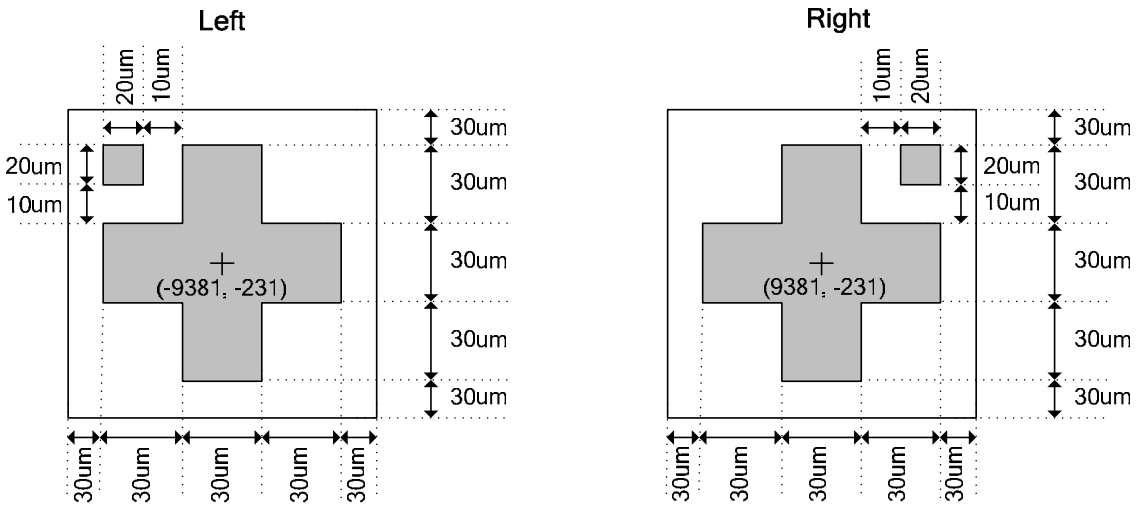
14.5. Alignment Mark

--Alignment Mark coordinate

Left (-9381, -231)

Right (9381, -231)

--Alignment Mark size



15. COG PRODUCTS MANUFACTURING GUIDELINES

15.1. Purpose:

The purpose of this specification is to identify ACF bonding process, so that customers can use properly ACF and Chip during the assembly.

15.2. Scope:

ACF bonding process

15.3. Noun definition

15.3.1. COG: Chip on Glass

15.3.2. ACF (Anisotropic Cunductive Film): .ACF is a functional adhesive tape which is able to connect (conductivity, adhesion, insulation) multiterminals in one time.

15.3.3. CTE: Coefficient of thermal expansion

15.4. Responsibility unity:

ORISETECH Quality Assurance unity

15.5. Contents:

15.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

IPC-A-610: Acceptability of Electronic Assemblies

15.5.2. ACF Characteristics:

10.5.2.1 Three factors to achieve the connection: Temperature, Pressure, Time.

15.5.3. ACF process :

10.5.3.1 To use Low Temperature and Low stress ACF is recommended for thin chip as 300 um.

10.5.3.2 Warp issues may happen if customers do not use Low Temperature and Low stress ACF for long chip .And warp issues may induce chip broken after ACF bonding for the CTE mismatch of Glass and ACF and Chip.

10.5.3.3 To use 3um ACF is recommended for BUMP space is less than 13um.

10.5.3.4 To use Low temperature and long time bonding is recommended if delamination happens in edge of chip.

10.5.3.5 For fine pitch and thin chip (300 um) products, customer should review ACF bonding condition with ACF maker.

15.6. References:

*IPC:

http://www.ipc.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

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17. REVISION HISTORY

Date	Revision #	Description	Page
DEC. 28, 2009	0.5	1. Add Vci condition with Vci=2.5V	5
		2. Add LEDON description when this pin is not in use.	9
		3. Add LEDPWM description when this pin is not in use	9
		4. Remove Description for Capacitor connection pins under BT[2:0] = [001] & [010] condition.	29
DEC. 03, 2009	0.4	1. Update Ordering Information & Pad Assignment & Pad Dimension.	5, 83
OCT. 01, 2009	0.3	1. Revise block diagram.	6
		2. Revise charge pump and power supply signal description.	9
		3. Revise misc. signal description.	10
		4. Remove SM setting.	14
		5. Revise Table 6-7	16
		6. Revise Table 6-21, RTNE setting fix error.	22-23
		7. Revise Table 6-28, AP[2:0] setting value.	29
		8. Revise Table 6-29, summarized the function of BT2-0 setting	29
		9. Rename VCIOUT to VCI1	30
		10. Revise DC12-10 setting and DC 02-00 setting.	30
		11. Remove commands R107h , R110h	33
		12. Revise chapter 10 “Power management system “	61-63
		13. Revise chapter 11 “Application circuit “	64
		14. Revise Power off sequence diagram.	73
		15. Revise chip size, bump hardness and bump height.	81
		16. Revise dummy pad name.	82
AUG. 05, 2009	0.2	Add CABC function	25-27
APR. 07, 2009	0.1	Original	89